# MX29F002/002N

## 2M-BIT [256K x 8] CMOS FLASH MEMORY

## FEATURES

- 262,144x 8 only
- Fast access time: 55/70/90/120ns
- Low power consumption
  - 30mA maximum active current(5MHz)
  - 1uA typical standby current
- Programming and erasing voltage 5V ± 10%
- Command register architecture
  - Byte Programming (7us typical)
  - Sector Erase (16K-Byte x1, 8K-Byte x 2, 32K-Byte x1, and 64K-Byte x 3)
- Auto Erase (chip & sector) and Auto Program
  - Automatically erase any combination of sectors or the whole chip with Erase Suspend capability.
  - Automatically programs and verifies data at specified address
- Erase Suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation.
- Status Reply
  - $\overline{\text{Data}}$ polling & Toggle bit for detection of program and erase cycle completion.
- Sector protection
  - Hardware method to disable any combination of sectors from program or erase operations
  - Sector protect/unprotect for 5V only system or 5V/12V system
- 100,000 minimum erase/program cycles
- Latch-up protected to 100mA from -1 to VCC+1V
- Boot Code Sector Architecture
  - T = Top Boot Sector
  - B = Bottom Boot Sector
- Hardware $\overline{\text{RESET}}$ pin(only for 29F002T/B)
  - Resets internal state machine to read mode
- Low VCC write inhibit is equal to or less than 3.2V
- Package type:
  - 32-pin PDIP
  - 32-pin PLCC
  - 32-pin TSOP (Type 1)
- 20 years data retention

## GENERAL DESCRIPTION

The MX29F002T/B is a 2-mega bit Flash memory organized as 256K bytes of 8 bits only. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29F002T/B is packaged in 32-pin PDIP,PLCC and 32-pin TSOP(I). It is designed to be reprogrammed and erased in-system or in-standard EPROM programmers.

The standard MX29F002T/B offers access time as fast as 55ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29F002T/B has separate chip enable ($\overline{\text{CE}}$) and output enable ($\overline{\text{OE}}$) controls.

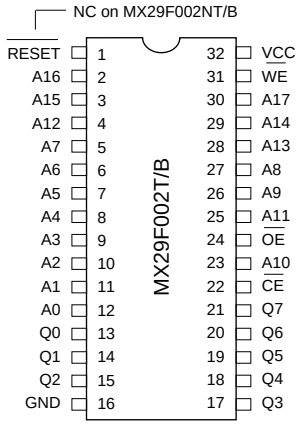
MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29F002T/B uses a command register to manage this functionality. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

MXIC's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29F002T/B uses a 5.0V ± 10% VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

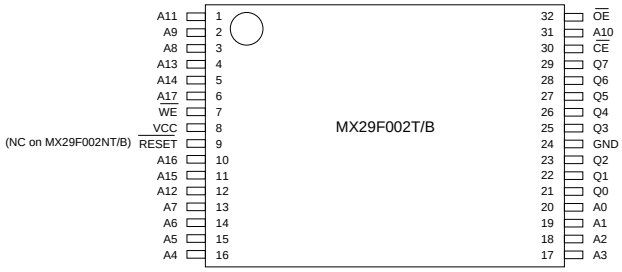
The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

## PIN CONFIGURATIONS

### 32 PDIP

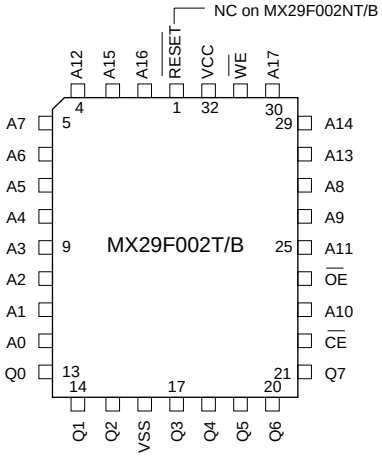



### 32 TSOP (TYPE 1)




**(NORMAL TYPE)**

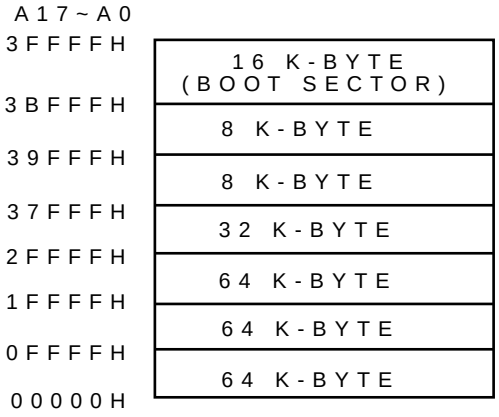
### 32 PLCC



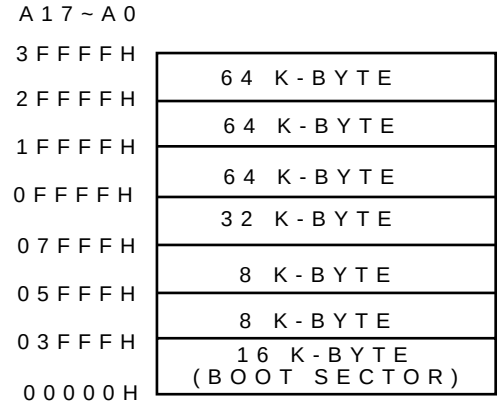

## PIN DESCRIPTION

| SYMBOL | PIN NAME |
|---|---|
| A0~A17 | Address Input |
| Q0~Q7 | Data Input/Output |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{WE}$ | Write Enable Input |
| $\overline{RESET}$ | Hardware Reset Pin/Sector Protect Unlock |
| $\overline{OE}$ | Output Enable Input |
| VCC | Power Supply Pin (+5V) |
| GND | Ground Pin |

## SECTOR STRUCTURE

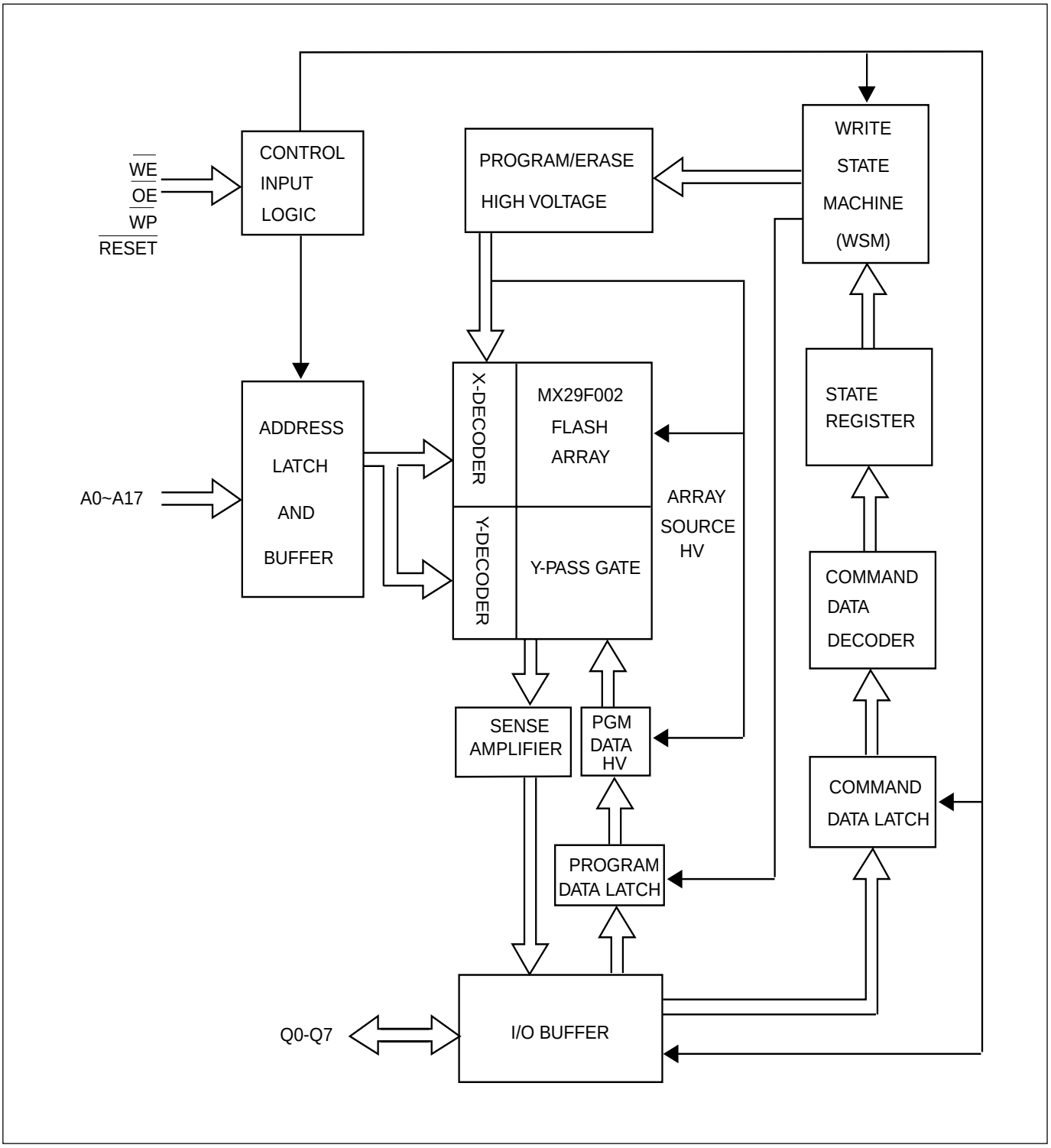



**MX29F002T Sector Architecture**




**MX29F002B Sector Architecture**

## BLOCK DIAGRAM



## AUTOMATIC PROGRAMMING

The MX29F002T/B is byte programmable using the Automatic Programming algorithm. The Automatic Programming algorithm does not require the system to time out or verify the data programmed. The typical chip programming time of the MX29F002T/B at room temperature is less than 3.5 seconds.

## AUTOMATIC CHIP ERASE

Typical erasure at room temperature is accomplished in less than 3 seconds. The device is erased using the Automatic Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are internally controlled by the device.

## AUTOMATIC SECTOR ERASE

The MX29F002T/B is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are internally controlled by the device.

## AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm requires the user to only write a program set-up commands include 2 unlock write cycle and A0H and a program command (program data and address). The device automatically times the programming pulse width, verifies the program, and counts the number of sequences. A status bit similar to DATA polling and a status bit toggling between consecutive read cycles, provides feedback to the user as to the status of the programming operation.

## AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, verifies the erase, and counts the number of sequences. A status bit similar to DATA polling and status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE .

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29F002T/B electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

## TABLE1. SOFTWARE COMMAND DEFINITIONS

| Command | Bus | First Bus Cycle | | Second Bus Cycle | | Third Bus Cycle | | Fourth Bus Cycle | | Fifth Bus Cycle | | Sixth Bus Cycle | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Cycle | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Reset | 1 | XXXH | F0H | | | | | | | | | | |
| Read | 1 | RA | RD | | | | | | | | | | |
| Read Silicon ID | 4 | 555H | AAH | 2AAH | 55H | 555H | 90H | ADI | DDI | | | | |
| Sector Protect Verification | 4 | 555H | AAH | 2AAH | 55H | 555H | 90H | (SA) (X02H) | 00H 01H | | | | |
| Porgram | 4 | 555H | AAH | 2AAH | 55H | 555H | A0H | PA | PD | | | | |
| Chip Erase | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 10H |
| Sector Erase | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | SA | 30H |
| Sector Erase Suspend | 1 | XXXH | B0H | | | | | | | | | | |
| Sector Erase Resume | 1 | XXXH | 30H | | | | | | | | | | |
| Unlock for sector protect/unprotect | 6 | 555H | AAH | 2AAH | 55H | 555H | 80H | 555H | AAH | 2AAH | 55H | 555H | 20H |

Note:
1. ADI = Address of Device identifier; A1=0,A0 =0 for manufacture code,A1=0, A0 =1 for device code (Refer to Table 3).
   DDI = Data of Device identifier : C2H for manufacture code, 00B0h/0034h for device code.
   X = X can be VIL or VIH
   RA=Address of memory location to be read.
   RD=Data to be read at location RA.
2. PA = Address of memory location to be programmed.
   PD = Data to be programmed at location PA.
   SA = Address to the sector to be erased.
3. The system should generate the following address patterns: 555H or 2AAH to Address A0~A10. Address bit A11~A17=X=Don't care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequence may be initiated with A11~A17 in either state.
4. For Sector Protect Verification Operation : If read out data is 01H, it means the sector has been protected. If read out data is 00H, it means the sector is still not being protected.

## COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 1 defines the valid register command sequences. Note that the Erase Suspend (B0H) and Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device(when applicable).

## TABLE 2. MX29F002T/B BUS OPERATION

| Pins / Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | A0 | A1 | A6 | A9 | Q0~Q7 |
|---|---|---|---|---|---|---|---|---|
| Read Silicon ID Manfacturer Code(1) | L | L | H | L | L | X | $V_{ID}$(2) | C2H |
| Read Silicon ID Device Code(1) | L | L | H | H | L | X | $V_{ID}$(2) | B0h/34h |
| Read | L | L | H | A0 | A1 | A6 | A9 | $D_{OUT}$ |
| Standby | H | X | X | X | X | X | X | HIGH Z |
| Output Disable | L | H | H | X | X | X | X | HIGH Z |
| Write | L | H | L | A0 | A1 | A6 | A9 | $D_{IN}$(3) |
| Sector Protect with 12V system(6) | L | $V_{ID}$(2) | L | X | X | L | $V_{ID}$(2) | X |
| Chip Unprotect with 12V system(6) | L | $V_{ID}$(2) | L | X | X | H | $V_{ID}$(2) | X |
| Verify Sector Protect with 12V system | L | L | H | X | H | X | $V_{ID}$(2) | Code(5) |
| Sector Protect without 12V system (6) | L | H | L | X | X | L | H | X |
| Chip Unprotect without 12V system (6) | L | H | L | X | X | H | H | X |
| Verify Sector Protect/Unprotect without 12V system (7) | L | L | H | X | H | X | H | Code(5) |
| Reset | X | X | X | X | X | X | X | HIGH Z |

**NOTES:**

1. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 1.
2. VID is the Silicon-ID-Read high voltage, 11.5V to 12.5V.
3. Refer to Table 1 for valid Data-In during a write operation.
4. X can be VIL or VIH.
5. Code=00H means unprotected.
   Code=01H means protected.
   A17~A13=Sector address for sector protect.
6. Refer to sector protect/unprotect algorithm and waveform.
   Must issue "unlock for sector protect/unprotect" command before "sector protect/unprotect without 12V system" command.
7. The "verify sector protect/unprotect without 12V sysytem" is only following "Sector protect/unprotect without 12V system" command.

## READ/RESET COMMAND

The read or reset operation is initiated by writing the read/ reset command sequence into the command register. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the command register contents are altered.

If program-fail or erase-fail happen, the write of F0H will reset the device to abort the operation. A valid command must then be written to place the device in the desired state.

## SILICON-ID-READ COMMAND

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

The MX29F002T/B contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL, A0=VIL retrieves the manufacturer code of C2H. A read cycle with A1=VIL, A0=VIH returns the device code of B0h for MX29F002T, 34h for MX29F002B.

## SET-UP AUTOMATIC CHIP/SECTOR ERASE COMMANDS

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H.

The Automatic Chip Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Chip Erase. Upon executing the Automatic Chip Erase, the device will automatically program and verify the entire memory for an all-zero data pattern. When the device is automatically verified to contain an all-zero pattern, a self-timed chip erase and verify begin. The erase and verify operations are completed when the data on Q7 is "1" at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Chip Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array(no erase verify command is required).

If the Erase operation was unsuccessful, the data on Q5 is "1"(see Table 4), indicating the erase operation exceed internal timing limit.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode.

### TABLE 3. EXPANDED SILICON ID CODE

| Pins | A0 | A1 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Code(Hex)Code |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Manufacture code** | VIL | VIL | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2H |
| **Device code for MX29F002T** | VIH | VIL | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h |
| **Device code for MX29F002B** | VIH | VIL | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34h |
| **Sector Protection** | X | VIH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01H (Protected) |
| **Verification** | X | VIH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00H (Unprotected) |

## SET-UP AUTOMATIC SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system does not require to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verification begin. The erase and verification operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system does not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command-80H. Two more "unlock" write cycles are then followed by the sector erase command-30H. The sector address is latched on the falling edge of $\overline{WE}$, while the command(data) is latched on the rising edge of $\overline{WE}$. Sector addresses selected are loaded into internal register on the sixth falling edge of $\overline{WE}$. Each successive sector load cycle started by the falling edge of $\overline{WE}$ must begin within 30us from the rising edge of the preceding $\overline{WE}$. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase (30H) or Erase Suspend (BOH) during the time-out period resets the device to read mode.

## ERASE SUSPEND

This command is only valid while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. Writing the Erase Suspend command during the Sector Erase time-out immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Read Memory Array, Erase Resume and Program commands. The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspendend program operation is complete, the system can once again read array data within non-suspended sectors.

## Table 4. Write Operation Status

| | Status | | Q7 Note1 | Q6 | Q5 Note2 | Q3 | Q2 |
|---|---|---|---|---|---|---|---|
| In Progress | Byte Program in Auto Program Algorithm | | $\overline{Q7}$ | Toggle | 0 | N/A | No Toggle |
| | Auto Erase Algorithm | | 0 | Toggle | 0 | 1 | Toggle |
| | Erase Suspended Mode | Erase Suspend Read (Erase Suspended Sector) | 1 | No Toggle | 0 | N/A | Toggle |
| | | Erase Suspend Read (Non-Erase Suspended Sector) | Data | Data | Data | Data | Data |
| | | Erase Suspend Program | $\overline{Q7}$ | Toggle | 0 | N/A | N/A |
| Exceeded Time Limits | Byte Program in Auto Program Algorithm | | $\overline{Q7}$ | Toggle | 1 | N/A | No Toggle |
| | Auto Erase Algorithm | | 0 | Toggle | 1 | 1 | Toggle |
| | Erase Suspend Program | | $\overline{Q7}$ | Toggle | 1 | N/A | N/A |

Note:
1. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
2. Q5 switches to '1' when an Auto Program or Auto Erase operation has exceeded the maximum timing limits. See "Q5:Exceeded Timing Limits " for more information.

## ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions.Another Erase Suspend command can be written after the chip has resumed erasing.

## SET-UP AUTOMATIC PROGRAM COMMANDS

To initiate Automatic Program mode, a three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the Automatic Program command A0H.

Once the Automatic Program command is initiated, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge, and data are internally latched on the rising edge of the $\overline{WE}$ pulse. The rising edge of $\overline{WE}$ also begins the programming operation. The system does not require to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin.

If the program opetation was unsuccessful, the data on Q5 is "1", indicating the program operation exceed internal timing limit. The automatic programming operation is completed when the data read on Q6 stops toggling for two consecutive read cycles and the data on Q7 and Q6 are equivalent to data written to these two bits, at which time the device returns to the Read mode(no program verify command is required).

## WRITE OPERATION STATUS

### $\overline{DATA}$ POLLING-Q7

The MX29F002T/B also features $\overline{Data}$ Polling as a method to indicate to the host system that the Automatic Program or Erase algorithms are either in progress or completed.

While the Automatic Programming algorithm is in operation, an attempt to read the device will produce the complement data of the data last written to Q7. Upon completion of the Automatic Program Algorithm an attempt to read the device will produce the true data last written to Q7. The $\overline{Data}$ Polling feature is valid after the rising edge of the fourth $\overline{WE}$ pulse of the four write pulse sequences for automatic program.

While the Automatic Erase algorithm is in operation, Q7 will read "0" until the erase operation is competed. Upon completion of the erase operation, the data on Q7 will read "1". The $\overline{Data}$ Polling feature is valid after the rising edge of the sixth $\overline{WE}$ pulse of six write pulse sequences for automatic chip/sector erase.

The $\overline{Data}$ Polling feature is active during Automatic Program/Erase algorithm or sector erase time-out.(see section Q3 Sector Erase Timer)

### Q6:Toggle BIT I

The MX29F002T/B features a "Toggle Bit" as a method to indicate to the host system that the Auto Program/Erase algorithms are either in progress or completed.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7(see the subsection on Q7:$\overline{Data}$ Polling).

If a program address falls within a protected sector, Q6 toggles for approximately 2 us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

The Write Operation Status table shows the outputs for Toggle Bit I on Q6. Refer to the toggle bit algorithmg.

## Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively eraseing (that is, the Automatic Erase alorithm is in process), or whether that sector is erase-suspended. Toggle Bit I is valid after the rising edge of the final $\overline{WE}$ pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either $\overline{OE}$ or $\overline{CE}$ to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 4 to compare outputs for Q2 and Q6.

## Reading Toggle Bits Q6/ Q2

Refer to the toggle bit algorithm for the following discussion. Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfuly completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation(top of the toggle bit algorithm flow chart).

## Q5

## Exceeded Timing Limits

Q5 will indicate if the program or erase time has exceeded the specified limits(internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector maynot be reused, (other sectors are still functional and can be reused).

The Q5 time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

## Q3

### Sector Erase Timer

After the completion of the initial sector erase command sequence th sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If Q3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

## DATA PROTECTION

The MX29F002T/B is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

## WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns(typical) on $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

## LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH or $\overline{WE}$ = VIH. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

## POWER SUPPLY DECOUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

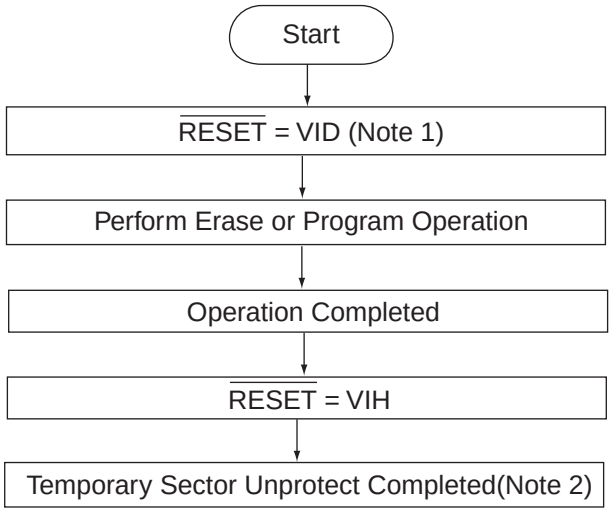
## SECTOR PROTECTION WITH 12V SYSTEM

The MX29F002T/B features hardware sector protection. This feature will disable both program and erase operations for these sectors protected. To activate this mode, the programming equipment must force VID on address pin A9 and control pin $\overline{OE}$, (suggest VID = 12V) A6 = VIL and $\overline{CE}$ = VIL.(see Table 2) Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge. Please refer to sector protect algorithm and waveform.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 ( with $\overline{CE}$ and $\overline{OE}$ at VIL and $\overline{WE}$ at VIH. When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses,except for A1, are in "don't care" state. Address locations with A1 = VIL are reserved to read manufacturer and device codes.(Read Silicon ID)

It is also possible to determine if the sector is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

## Temporary Sector Unprotect Operation (For 29F002T/B only)




Note : 1. All protected sectors are temporary unprotected.
VID=11.5V~12.5V

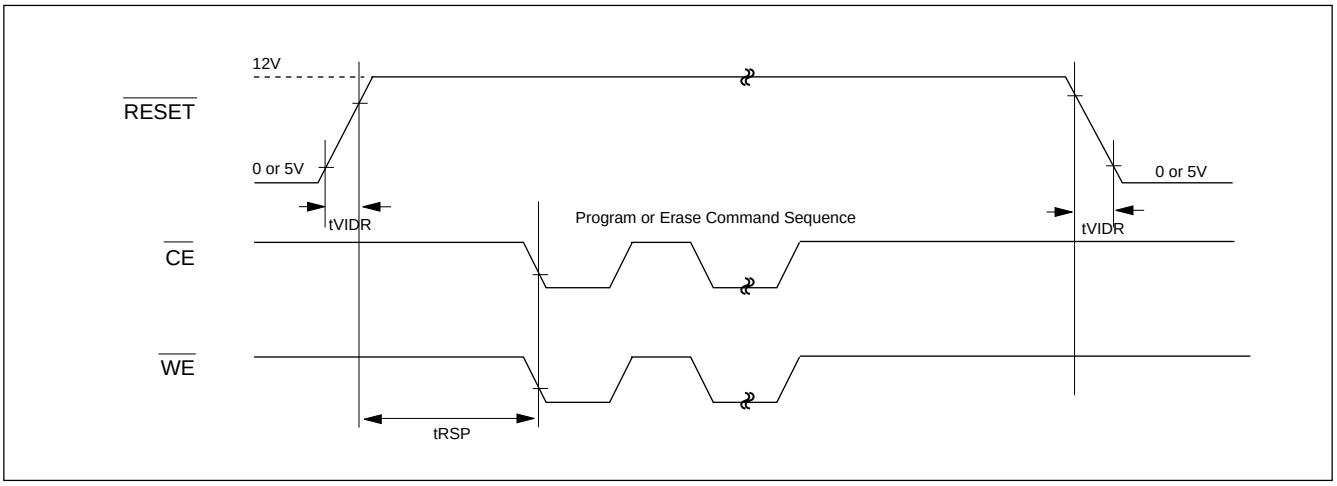
2. All previously protected sectors are protected again.

## TEMPORARY SECTOR UNPROTECT

| Parameter Std. | Description | Test Setup | AllSpeed Options | Unit |
|---|---|---|---|---|
| tVIDR | VID Rise and Fall Time (See Note) | Min | 500 | ns |
| tRSP | $\overline{\text{RESET}}$ Setup Time for Temporary Sector Unprotect | Min | 4 | us |

Note:
Not 100% tested

## Temporary Sector Unprotect Timing Diagram(For 29F002T/B only)

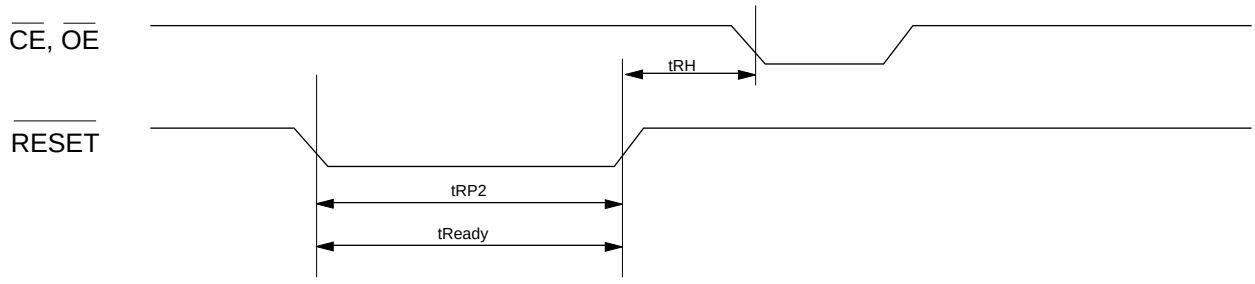


## AC CHARACTERISTICS

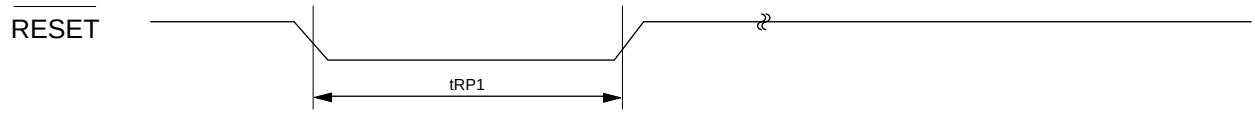
| Parameter Std | Description | Test Setup | All Speed Options | Unit |
|---|---|---|---|---|
| tREADY | $\overline{\text{RESET}}$ PIN Low (Not During Automatic Algorithms) to Read or Write (See Note) | MAX | 500 | ns |
| tRP1 | $\overline{\text{RESET}}$ Pulse Width (During Automatic Algorithms) | MIN | 10 | us |
| tRP2 | $\overline{\text{RESET}}$ Pulse Width (NOT During Automatic Algorithms) | MIN | 500 | ns |
| tRH | $\overline{\text{RESET}}$ High Time Before Read(See Note) | MIN | 0 | ns |

Note:
Not 100% tested

## $\overline{\text{RESET}}$ TIMING WAVFORM (For 29F002T/B only)




Reset Timing NOT during Automatic Algorithms




Reset Timing during Automatic Algorithms

## CHIP UNPROTECT WITH 12V SYSTEM

The MX29F002T/B also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin $\overline{OE}$ and address pin A9. The $\overline{CE}$ pins must be set at VIL. Pins A6 must be set to VIH.(see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated on the rising edge.

It is also possible to determine if the chip is unprotected in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs(Q0-Q7) for an unprotected sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

## SECTOR PROTECTION WITHOUT 12V SYSTEM

The MX29F002T/B also feature a hardware sector protection method in a system without 12V power suppply. The programming equipment do not need to supply 12 volts to protect sectors. The details are shown in sector protect algorithm and waveform.

## CHIP UNPROTECT WITHOUT 12V SYSTEM

The MX29F002T/B also feature a hardware chip unprotection method in a system without 12V power supply. The programming equipment do not need to supply 12 volts to unprotect all sectors. The details are shown in chip unprotect algorithm and waveform.

## POWER-UP SEQUENCE

The MX29F002T/B powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two-step command sequence. Vpp and Vcc power up sequence is not required.

## ABSOLUTE MAXIMUM RATINGS

| RATING | VALUE |
|---|---|
| Ambient Operating Temperature | 0°C to 70°C |
| Storage Temperature | -65°C to 125°C |
| Applied Input Voltage | -0.5V to 7.0V |
| Applied Output Voltage | -0.5V to 7.0V |
| VCC to Ground Potential | -0.5V to 7.0V |
| A9 | -0.5V to 13.5V |

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

## DC/AC Operating Conditions for Read/Programming/Erase Operation

| | | MX29F002/002N | | | |
|---|---|---|---|---|---|
| | | -55 | -70 | -90 | -12 |
| Operating Temperature | Commercial | 0°C to 70°C | 0°C to 70°C | 0°C to 70°C | 0°C to 70°C |
| | Industrial | | -40°C to 85°C | -40°C to 85°C | -40°C to 85°C |
| Vcc Power Supply | | 5V±5% | 5V±10% | 5V±10% | 5V±10% |

## CAPACITANCE TA = 25°C, f = 1.0 MHz

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| CIN1 | Input Capacitance | | | 8 | pF | VIN = 0V |
| CIN2 | Control Pin Capacitance | | | 12 | pF | VIN = 0V |
| COUT | Output Capacitance | | | 12 | pF | VOUT = 0V |

## READ OPERATION

### DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| ILI | Input Leakage Current | | | 1(Note 3) | uA | VIN = GND to VCC |
| ILO | Output Leakage Current | | | 10 | uA | VOUT = GND to VCC |
| ISB1 | Standby VCC current | | | 1 | mA | $\overline{CE}$ = VIH |
| ISB2 | | | 1 | 5 | uA | $\overline{CE}$ = VCC + 0.3V |
| ICC1 | Operating VCC current | | | 30(Note 4) | mA | IOUT = 0mA, f=5MHz |
| ICC2 | | | | 50 | mA | IOUT = 0mA, f=10MHz |
| VIL | Input Low Voltage | -0.3(NOTE 1) | | 0.8 | V | |
| VIH | Input High Voltage | 2.0 | | VCC + 0.3 | V | |
| VOL | Output Low Voltage | | | 0.45 | V | IOL = 2.1mA |
| VOH1 | Output High Voltage(TTL) | 2.4 | | | V | IOH = -2mA |
| VOH2 | Output High Voltage(CMOS) | VCC-0.4 | | | V | IOH = -100uA, VCC=VCC MIN |

NOTES:
1. VIL min. = -1.0V for pulse width is equal to or less than 50 ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20 ns.
2. VIH max. = VCC + 1.5V for pulse width is equal to or less than 20 ns.
   If VIH is over the specified maximum value, read operation cannot be guaranteed.
3. ILI=10uA for Industrial grade.
4. ICC1=45mA for Industrial grade.

## AC CHARACTERISTICS

| | | 29F002T/B-55 | | 29F002T/B-70 | | | |
|---|---|---|---|---|---|---|---|
| **SYMBOL** | **PARAMETER** | **MIN.** | **MAX.** | **MIN.** | **MAX.** | **UNIT** | **CONDITION** |
| tACC | Address to Output Delay | | 55 | | 70 | ns | $\overline{CE}$=$\overline{OE}$=VIL |
| tCE | $\overline{CE}$ to Output Delay | | 55 | | 70 | ns | $\overline{OE}$=VIL |
| tOE | $\overline{OE}$ to Output Delay | | 25 | | 30 | ns | $\overline{CE}$=VIL |
| tDF | $\overline{OE}$ High to Output Float (Note1) | 0 | 20 | 0 | 20 | ns | $\overline{CE}$=VIL |
| tOH | Address to Output hold | 0 | | 0 | | ns | $\overline{CE}$=$\overline{OE}$=VIL |

| | | 29F002T/B-90 | | 29F002T/B-12 | | | |
|---|---|---|---|---|---|---|---|
| **SYMBOL** | **PARAMETER** | **MIN.** | **MAX.** | **MIN.** | **MAX.** | **UNIT** | **CONDITIONS** |
| tACC | Address to Output Delay | | 90 | | 120 | ns | $\overline{CE}$=$\overline{OE}$=VIL |
| tCE | $\overline{CE}$ to Output Delay | | 90 | | 120 | ns | $\overline{OE}$=VIL |
| tOE | $\overline{OE}$ to Output Delay | | 40 | | 50 | ns | $\overline{CE}$=VIL |
| tDF | $\overline{OE}$ High to Output Float (Note1) | 0 | 30 | 0 | 30 | ns | $\overline{CE}$=VIL |
| tOH | Address to Output hold | 0 | | 0 | | ns | $\overline{CE}$=$\overline{OE}$=VIL |

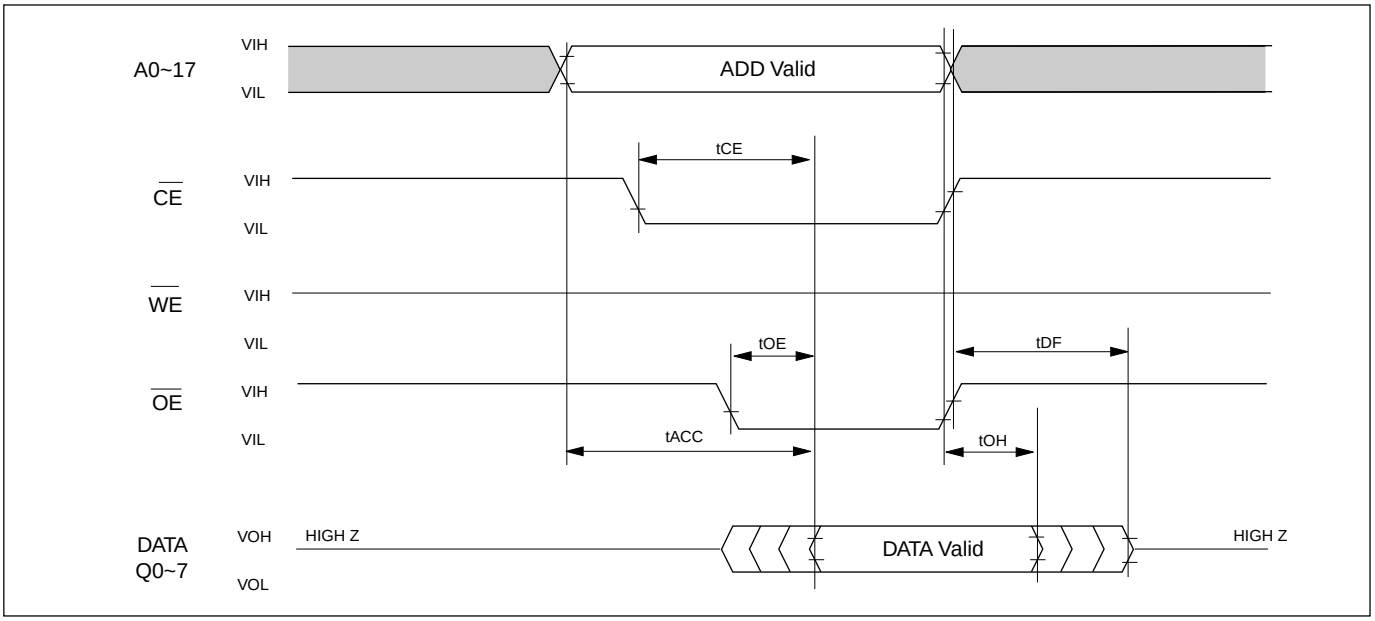
### TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V for 70ns max., 0V/3V for 55ns
- Input rise and fall times: ≤ 10ns for 70ns max.
  ≤ 5ns for 55ns
- Output load:
  1 TTL gate + 100pF (Including scope and jig) for 70ns max.
  1 TTL gate + 50pF (Including scope and jig) for 55ns speed grade
- Reference levels for measuring timing: 0.8V, 2.0V for 70ns max.
  : 1.5V for 55ns

**NOTE:**

1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

## READ TIMING WAVEFORMS



## COMMAND PROGRAMMING/DATA PROGRAMMING/ERASE OPERATION

### DC CHARACTERISTICS

| SYMBOL | PARAMETER | MIN. | TYP | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| ICC1 (Read) | Operating VCC Current | | | 30(Note 5) | mA | IOUT=0mA, f=5MHz |
| ICC2 | | | | 50 | mA | IOUT=0mA, F=10MHz |
| ICC3 (Program) | | | | 50 | mA | In Programming |
| ICC4 (Erase) | | | | 50 | mA | In Erase |
| ICCES | VCC Erase Suspend Current | | 2 | | mA | $\overline{CE}$=VIH, Erase Suspended |

**NOTES:**

1. VIL min. = -0.6V for pulse width is equal to or less than 20ns.
2. If VIH is over the specified maximum value, programming operation cannot be guranteed.
3. ICCES is specified with the device de-selected. If the device is read during erase suspend mode, current draw is the sum of ICCES and ICC1 or ICC2.
4. All current are in RMS unless otherwise noted.
5. ICC1(Read)=45mA for Industrial Grade.

## AC CHARACTERISTICS

| | | 29F002T/B-55(NOTE 2) | | |
|---|---|---|---|---|
| **SYMBOL** | **PARAMETER** | **MIN.** | **MAX.** | **UNIT CONDITIONS** |
| tOES | $\overline{OE}$ setup time | 0 | | ns |
| tCWC | Command programming cycle | 70 | | ns |
| tCEP | $\overline{WE}$ programming pulse width | 45 | | ns |
| tCEPH1 | $\overline{WE}$ programming pluse width High | 20 | | ns |
| tCEPH2 | $\overline{WE}$ programming pluse width High | 20 | | ns |
| tAS | Address setup time | 0 | | ns |
| tAH | Address hold time | 45 | | ns |
| tDS | Data setup time | 20 | | ns |
| tDH | Data hold time | 0 | | ns |
| tCESC | $\overline{CE}$ setup time before command write | 0 | | ns |
| tDF | Output disable time (Note 1) | | 20 | ns |
| tAETC | Total erase time in auto chip erase | 3(TYP.) | 24 | s |
| tAETB | Total erase time in auto sector erase | 1(TYP.) | 8 | s |
| tAVT | Total programming time in auto verify (Byte Program time) | 7 | 210 | us |
| tBAL | Sector address load time | 100 | | us |
| tCH | $\overline{CE}$ Hold Time | 0 | | ns |
| tCS | $\overline{CE}$ setup to $\overline{WE}$ going low | 0 | | ns |
| tVLHT | Voltge Transition Time | 4 | | us |
| tOESP | $\overline{OE}$ Setup Time to $\overline{WE}$ Active | 4 | | us |
| tWPP1 | Write pulse width for sector protect | 10 | | us |
| tWPP2 | Write pulse width for sector unprotect | 12 | | ms |

**NOTES:**

1.tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

2.The test conditin of MX29F002T/B-55 : VCC=5V ± 5%,CL=50pf,VIH/VIL=3.0V/0V
VOH/VOL=1.5V/1.5V,IOL=2mA,IOH=-2mA
TA= 0°C TO 70°C

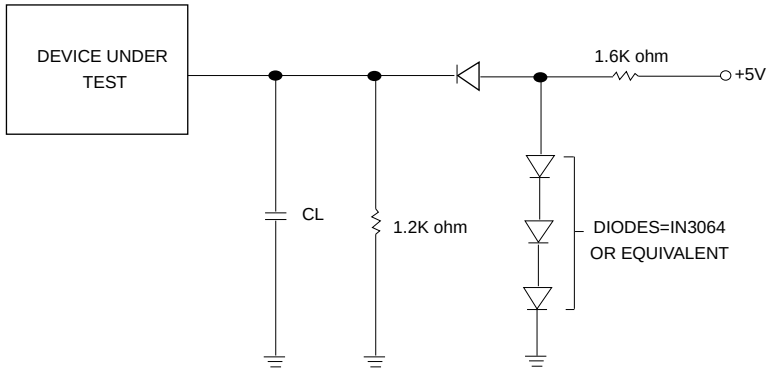
## AC CHARACTERISTICS

| | | 29F002T/B-70 | | 29F002T/B-90 | | 29F002T/B-12 | | | |
|---|---|---|---|---|---|---|---|---|---|
| **SYMBOL** | **PARAMETER** | **MIN.** | **MAX.** | **MIN.** | **MAX.** | **MIN.** | **MAX.** | **UNIT** | **CONDITIONS** |
| tOES | $\overline{OE}$ setup time | 0 | | 0 | | 0 | | ns | |
| tCWC | Command programming cycle | 70 | | 90 | | 120 | | ns | |
| tCEP | $\overline{WE}$ programming pulse width | 45 | | 45 | | 50 | | ns | |
| tCEPH1 | $\overline{WE}$ programming pluse width High | 20 | | 20 | | 20 | | ns | |
| tCEPH2 | $\overline{WE}$ programming pluse width High | 20 | | 20 | | 20 | | ns | |
| tAS | Address setup time | 0 | | 0 | | 0 | | ns | |
| tAH | Address hold time | 45 | | 45 | | 50 | | ns | |
| tDS | Data setup time | 30 | | 45 | | 50 | | ns | |
| tDH | Data hold time | 0 | | 0 | | 0 | | ns | |
| tCESC | $\overline{CE}$ setup time before command write | 0 | | 0 | | 0 | | ns | |
| tDF | Output disable time (Note 1) | | 30 | | 40 | | 40 | ns | |
| tAETC | Total erase time in auto chip erase | 3(TYP.) | 24 | 3(TYP.) | 24 | 3(TYP.) | 24 | s | |
| tAETB | Total erase time in auto sector erase | 1(TYP.) | 8 | 1(TYP.) | 8 | 1(TYP.) | 8 | s | |
| tAVT | Total programming time in auto verify (Byte Program time) | 7 | 210 | 7 | 210 | 7 | 210 | us | |
| tBAL | Sector address load time | 100 | | 100 | | 100 | | us | |
| tCH | $\overline{CE}$ Hold Time | 0 | | 0 | | 0 | | ns | |
| tCS | $\overline{CE}$ setup to $\overline{WE}$ going low | 0 | | 0 | | 0 | | ns | |
| tVLHT | Voltge Transition Time | 4 | | 4 | | 4 | | us | |
| tOESP | $\overline{OE}$ Setup Time to $\overline{WE}$ Active | 4 | | 4 | | 4 | | us | |
| tWPP1 | Write pulse width for sector protect | 10 | | 10 | | 10 | | us | |
| tWPP2 | Write pulse width for sector unprotect | 12 | | 12 | | 12 | | ms | |

**NOTES:**

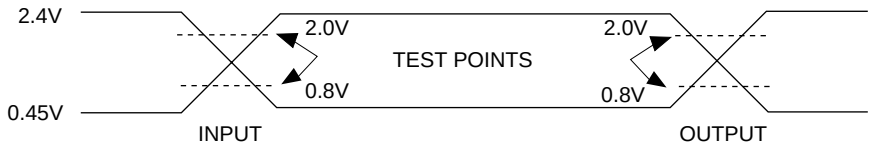
1. tDF defined as the time at which the output achieves the open circuit condition and data is no longer driven.

## SWITCHING TEST CIRCUITS



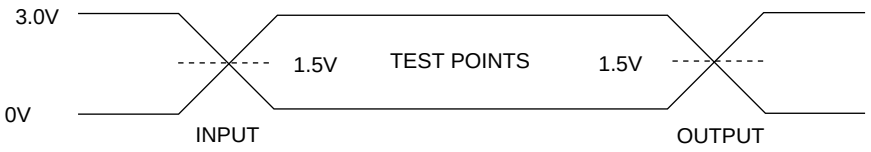

CL=100pF Including jig capacitance
CL=50pF for MX29F002T/B-55

## SWITCHING TEST WAVEFORMS(I) for speed grade 70ns max.



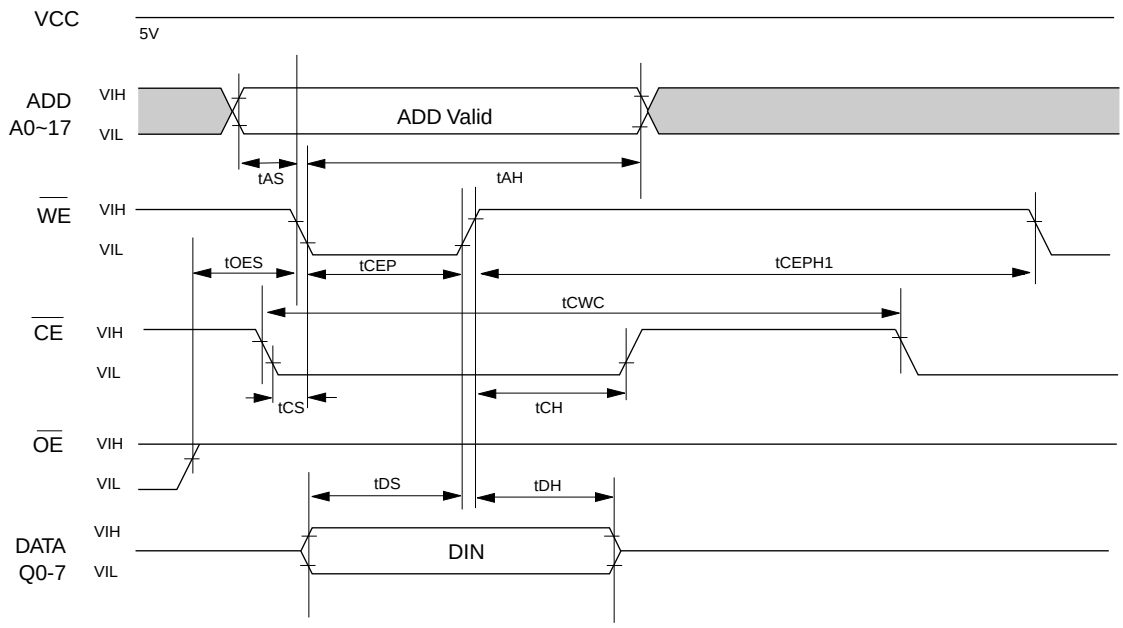

AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are equal to or less than 20ns.

## SWITCHING TEST WAVEFORMS(II) for speed grade 55ns(MX29F002T/B-55)




AC TESTING: Inputs are driven at 3.0V for a logic "1" and 0V for a logic "0".
Input pulse rise and fall times are < 5ns.

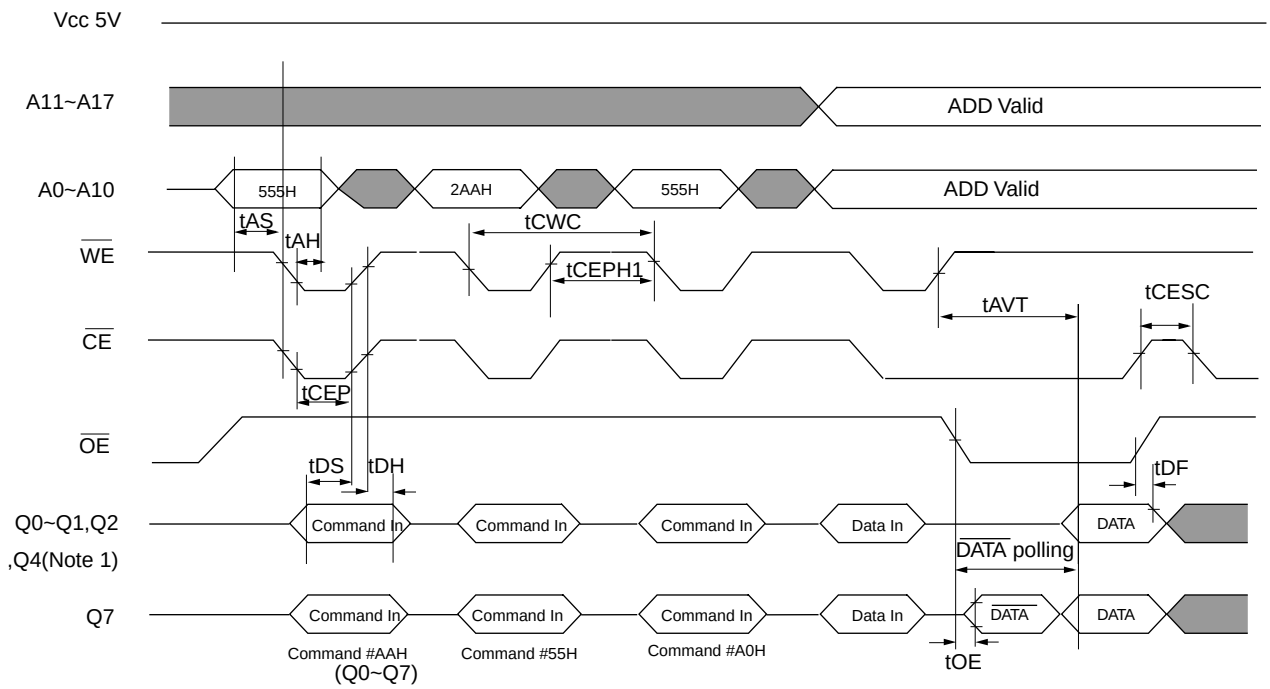
## COMMAND WRITE TIMING WAVEFORM



## AUTOMATIC PROGRAMMING TIMING WAVEFORM

One byte data is programmed. Verify in fast algorithm and additional programming by external control are not required because these operations are executed automatically by internal control circuit. Programming completion can be verified by $\overline{DATA}$ polling and toggle bit checking after automatic verification starts. Device outputs $\overline{DATA}$ during programming and DATA after programming on Q7.(Q6 is for toggle bit; see toggle bit, $\overline{DATA}$ polling, timing waveform)

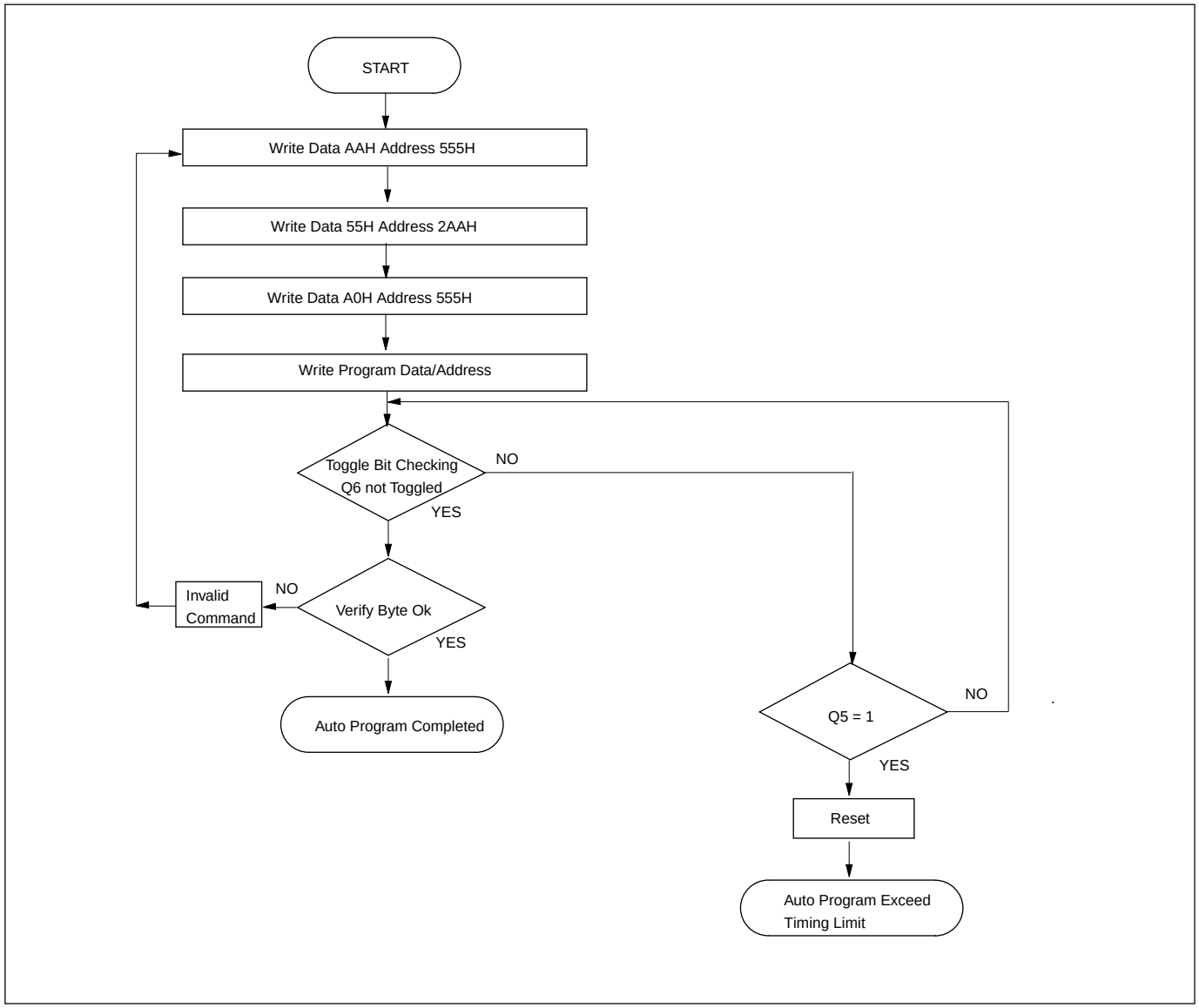
## AUTOMATIC PROGRAMMING TIMING WAVEFORM



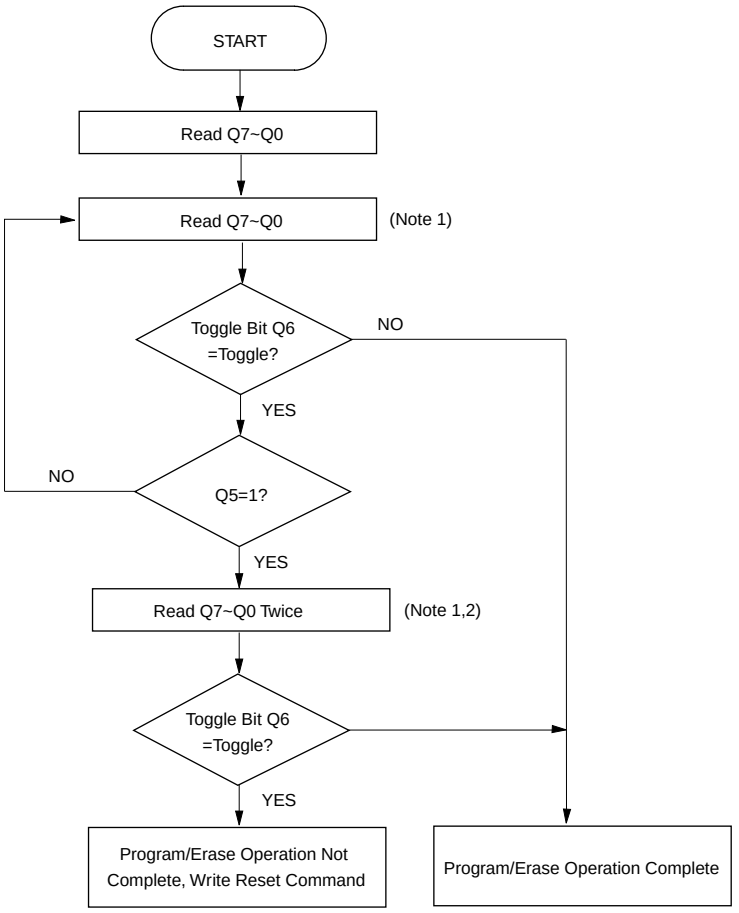

Notes:

(1). Q6:Toggle bit, Q5:Tin=Timing-limit bit, Q3: Time-out bit

## AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART



## TOGGLE BIT ALGORITHM

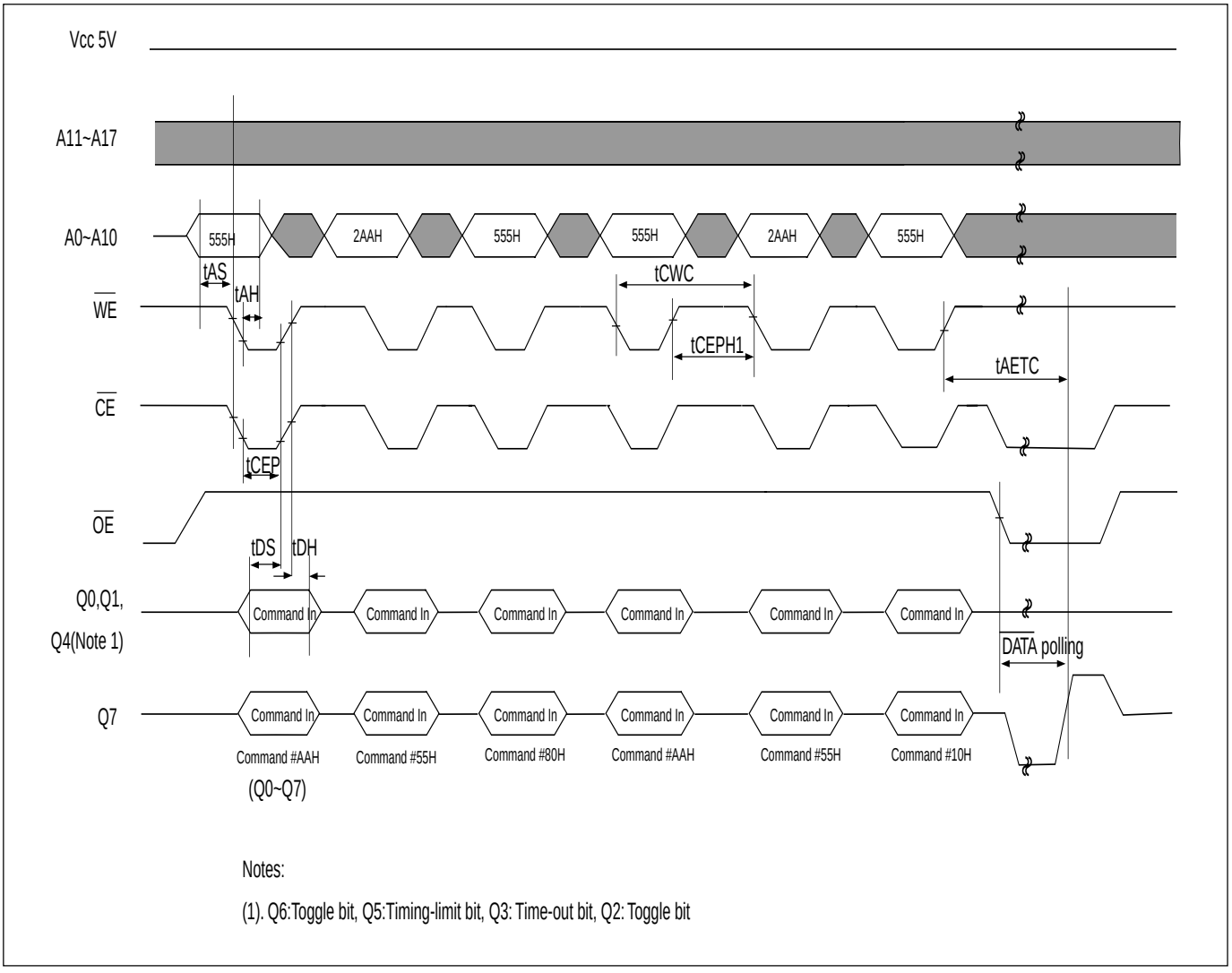



Note:
1. Read toggle bit Q6 twice to determine whether or not it is toggle. See test.
2. Recheck toggle bit Q6 because it may stop toggling as Q5 changes to "1". See test.

## AUTOMATIC CHIPE RASETIMING WAVEFORM

All data in chip are erased. External erase verify is not required because data is erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

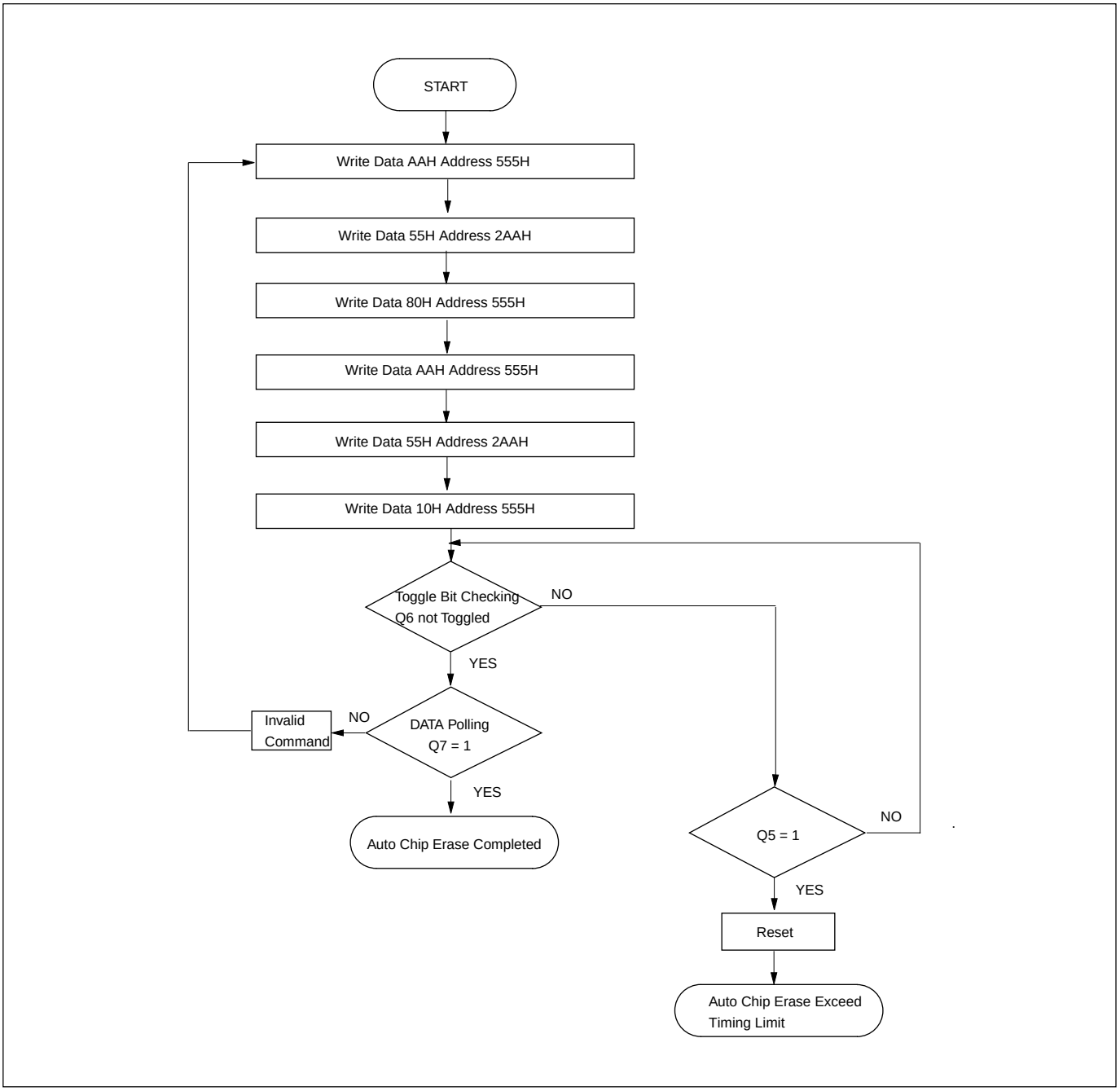
## AUTOMATIC CHIP ERASE TIMING WAVEFORM




Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

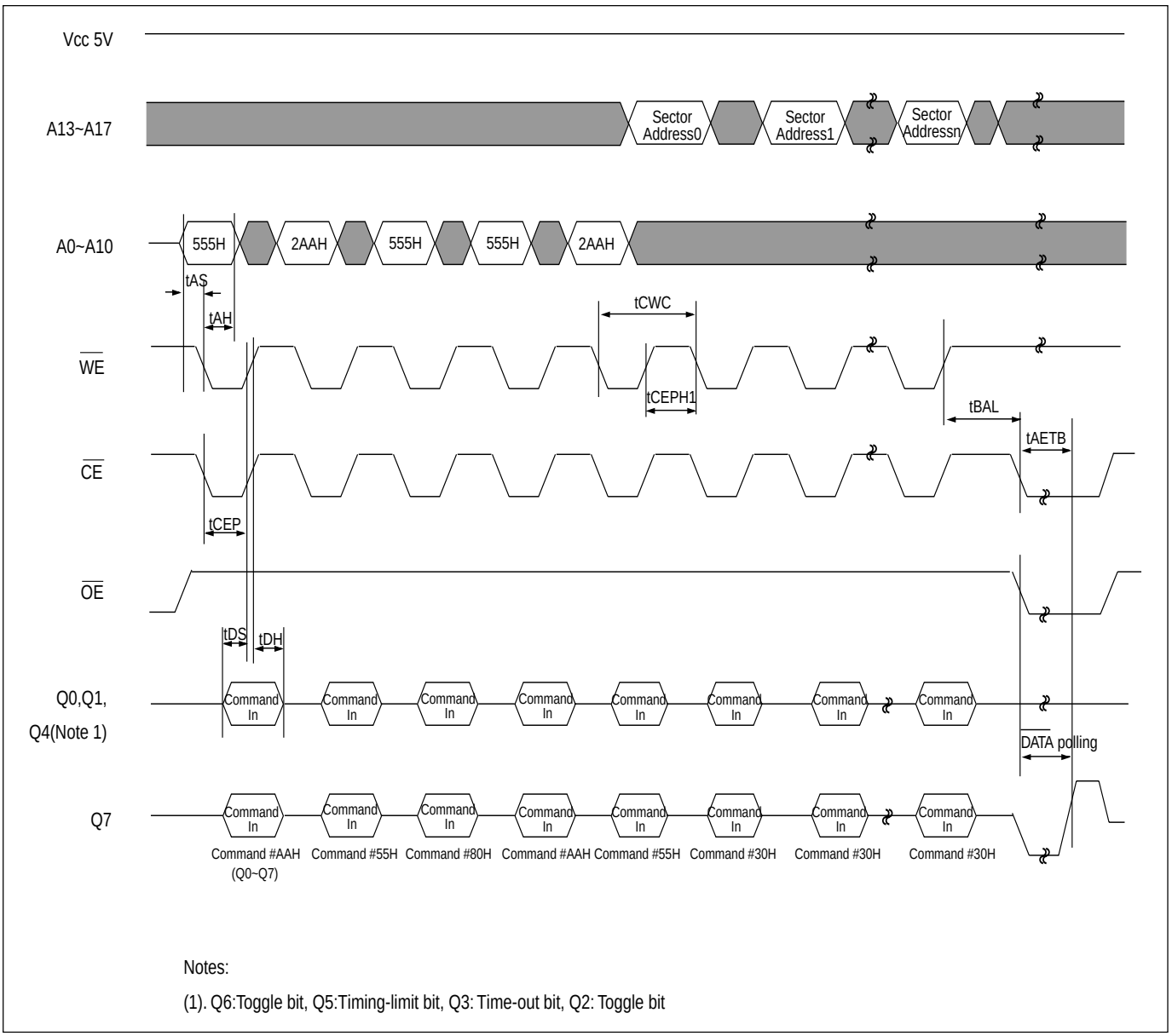
## AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART



## AUTOMATIC SECTOR ERASE TIMING WAVEFORM

Sector data indicated by A13 to A17 are erased. External erase verification is not required because data are erased automatically by internal control circuit. Erasure completion can be verified by DATA polling and toggle bit checking after automatic erase starts. Device outputs 0 during erasure and 1 after erasure on Q7.(Q6 is for toggle bit; see toggle bit, DATA polling, timing waveform)

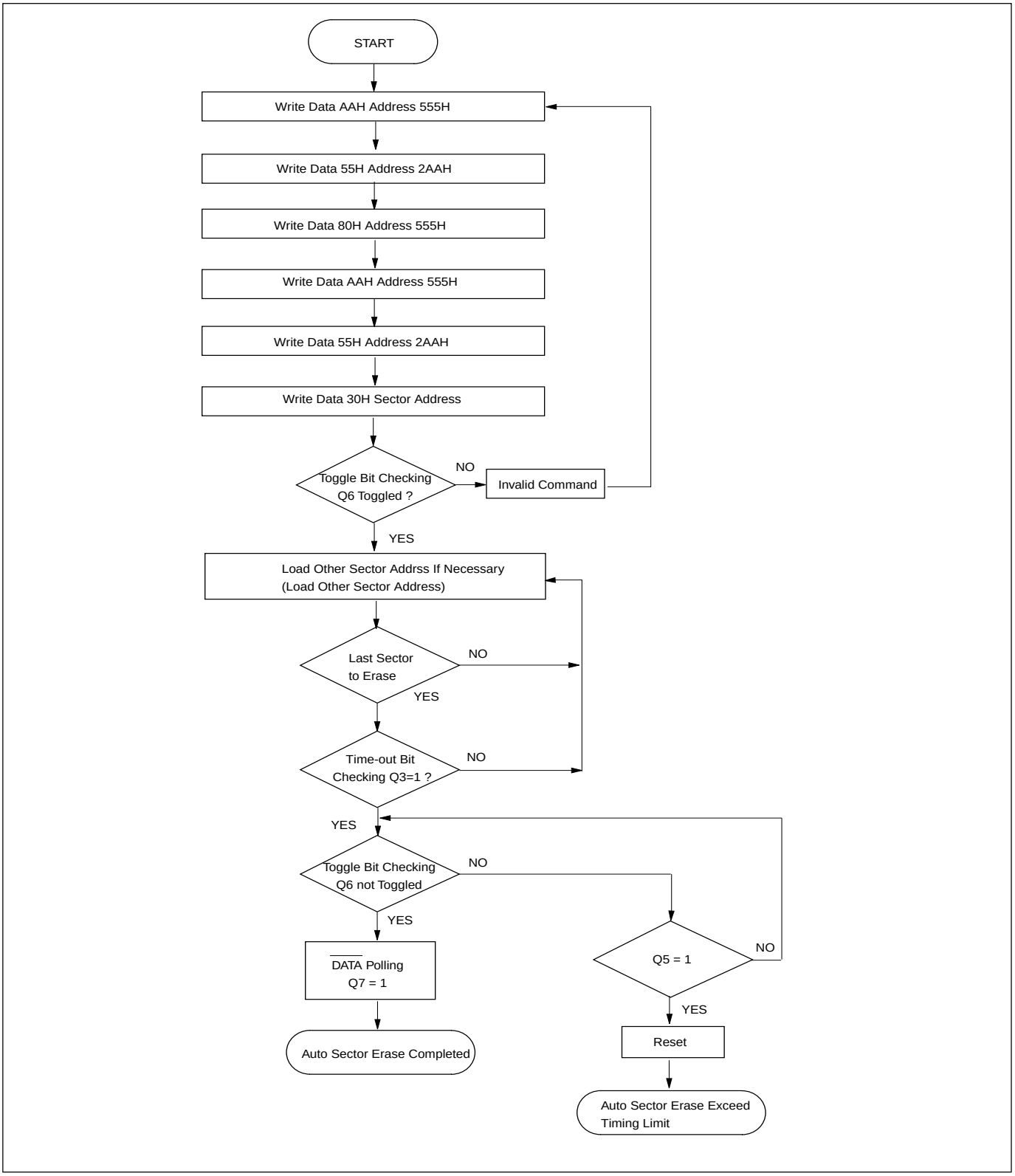
## AUTOMATIC SECTOR ERASE TIMING WAVEFORM



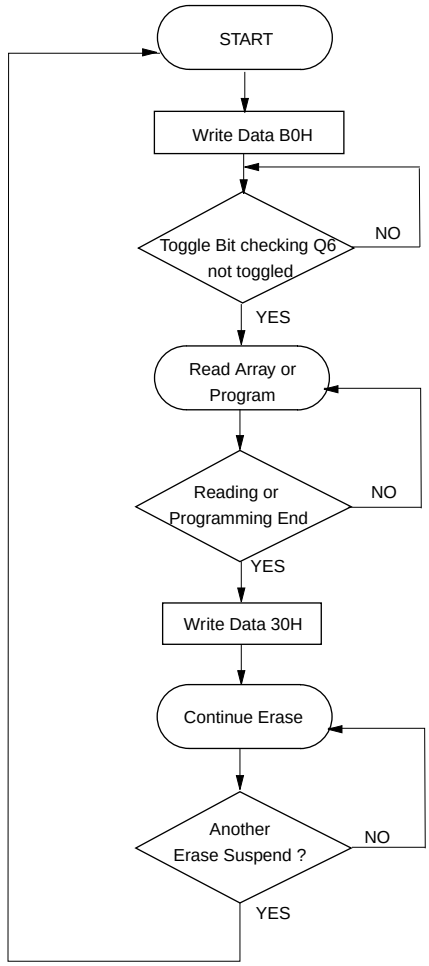

Notes:

(1). Q6:Toggle bit, Q5:Timing-limit bit, Q3: Time-out bit, Q2: Toggle bit

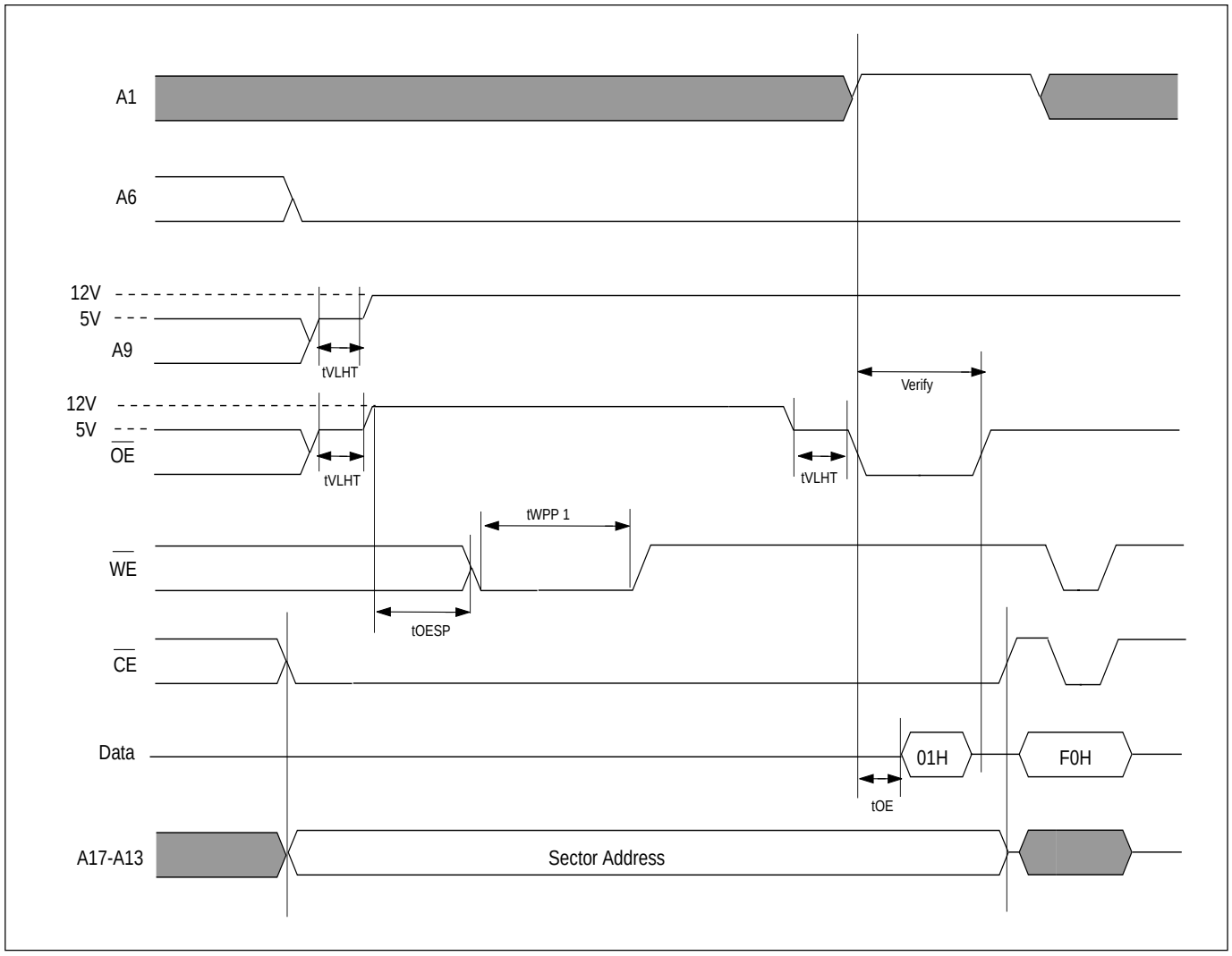
## AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART



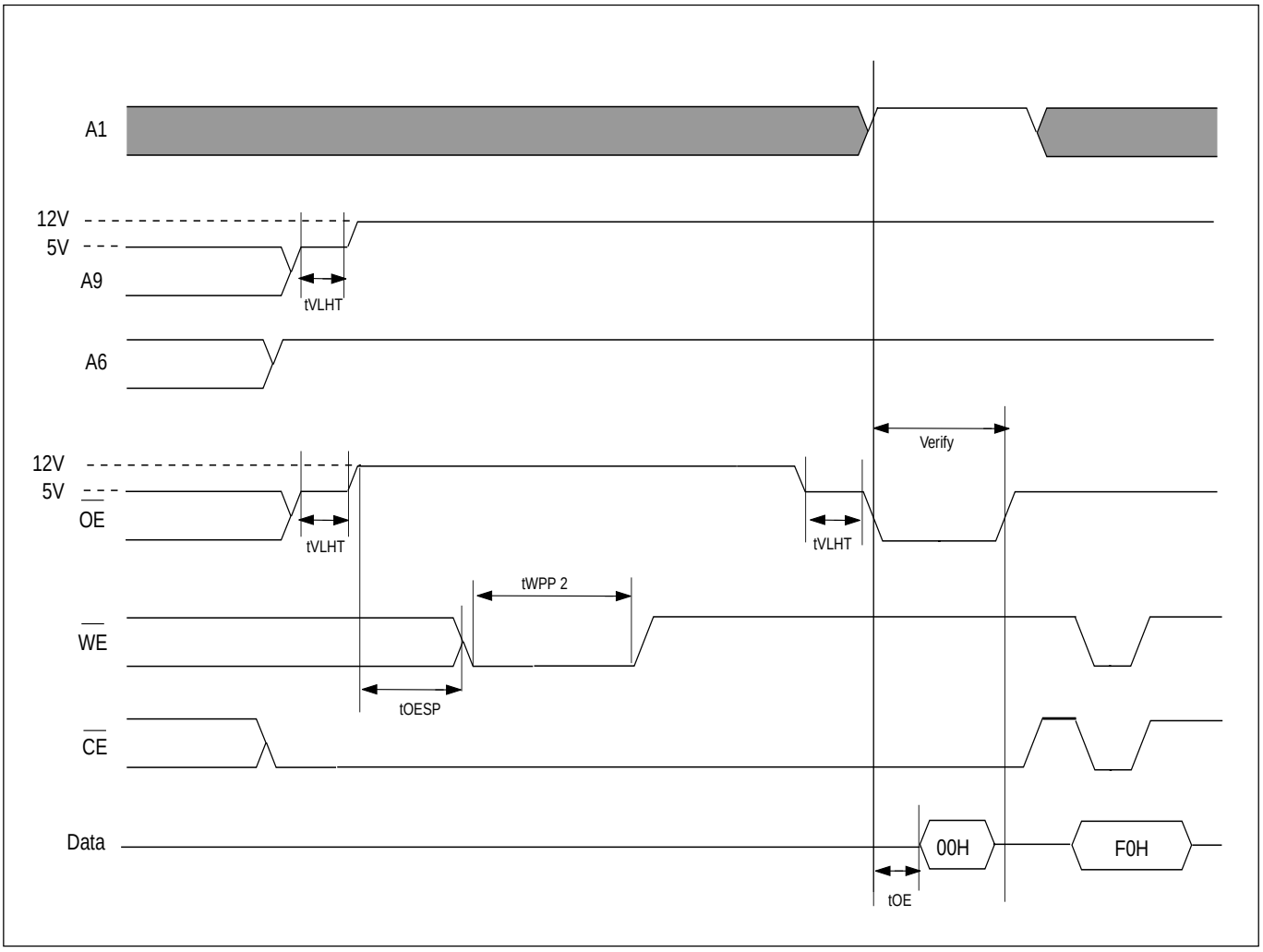
## ERASE SUSPEND/ERASE RESUME FLOWCHART



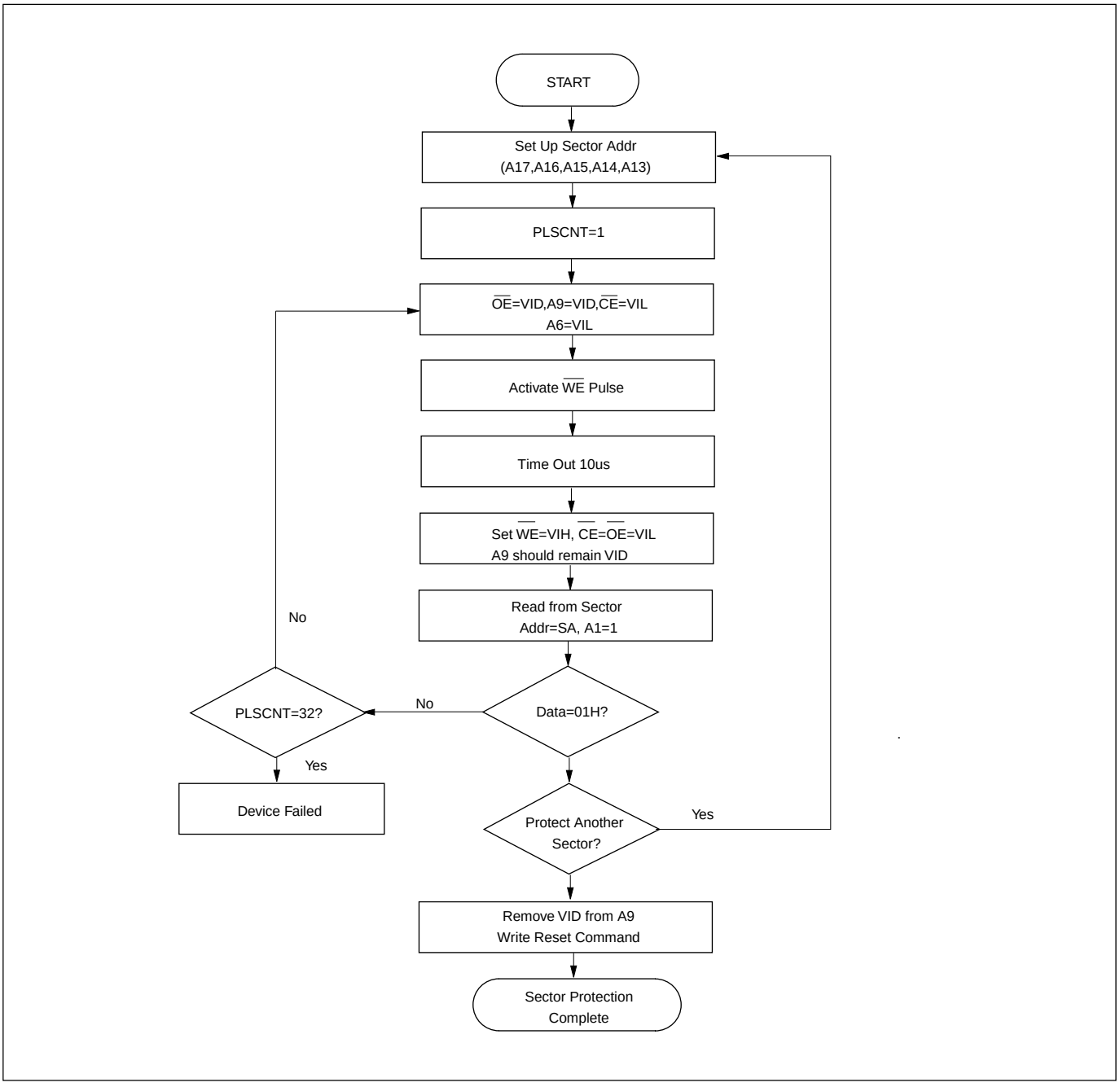
## TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITH 12V



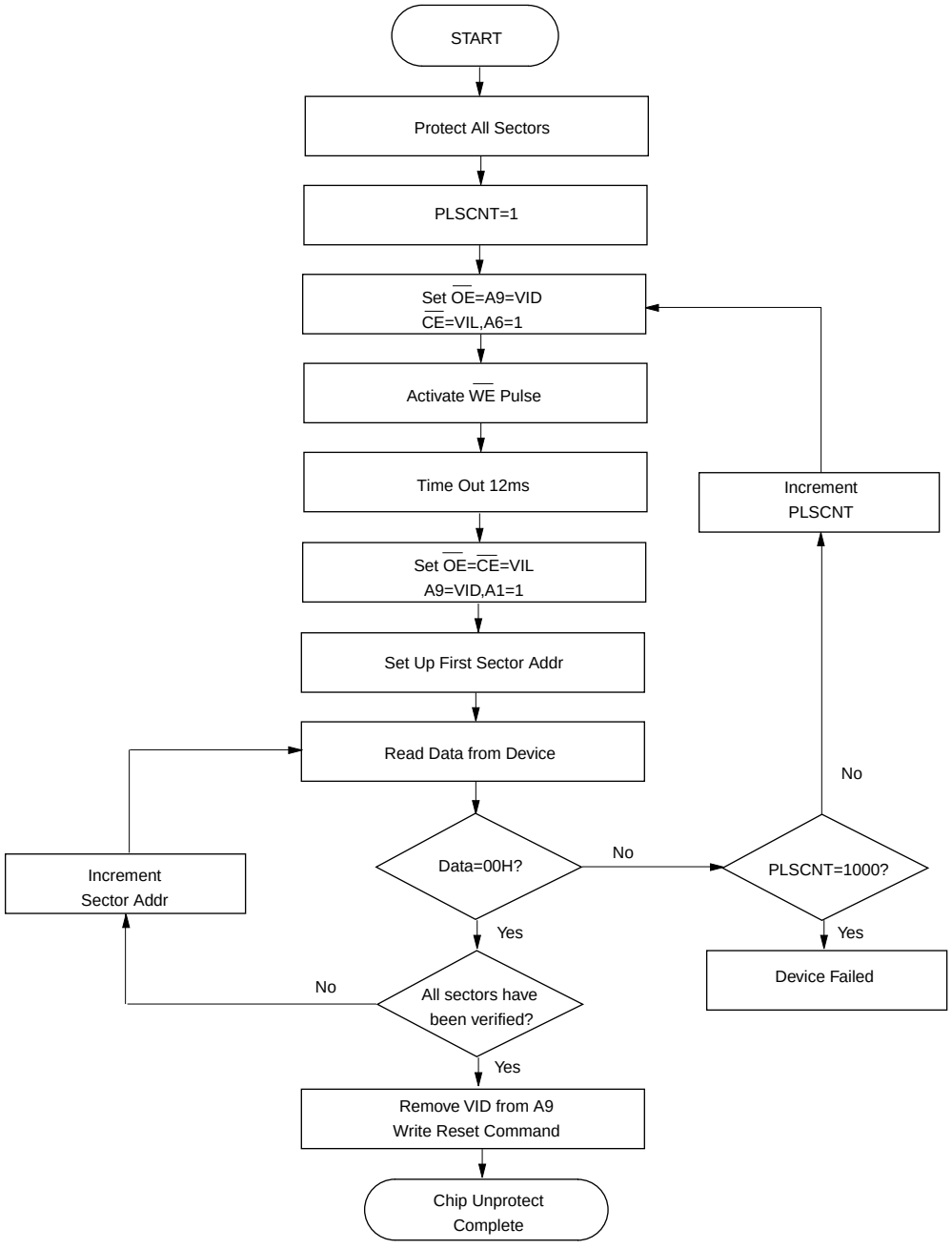
## TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITH 12V



## SECTOR PROTECTION ALGORITHM FOR SYSTEM WITH 12V

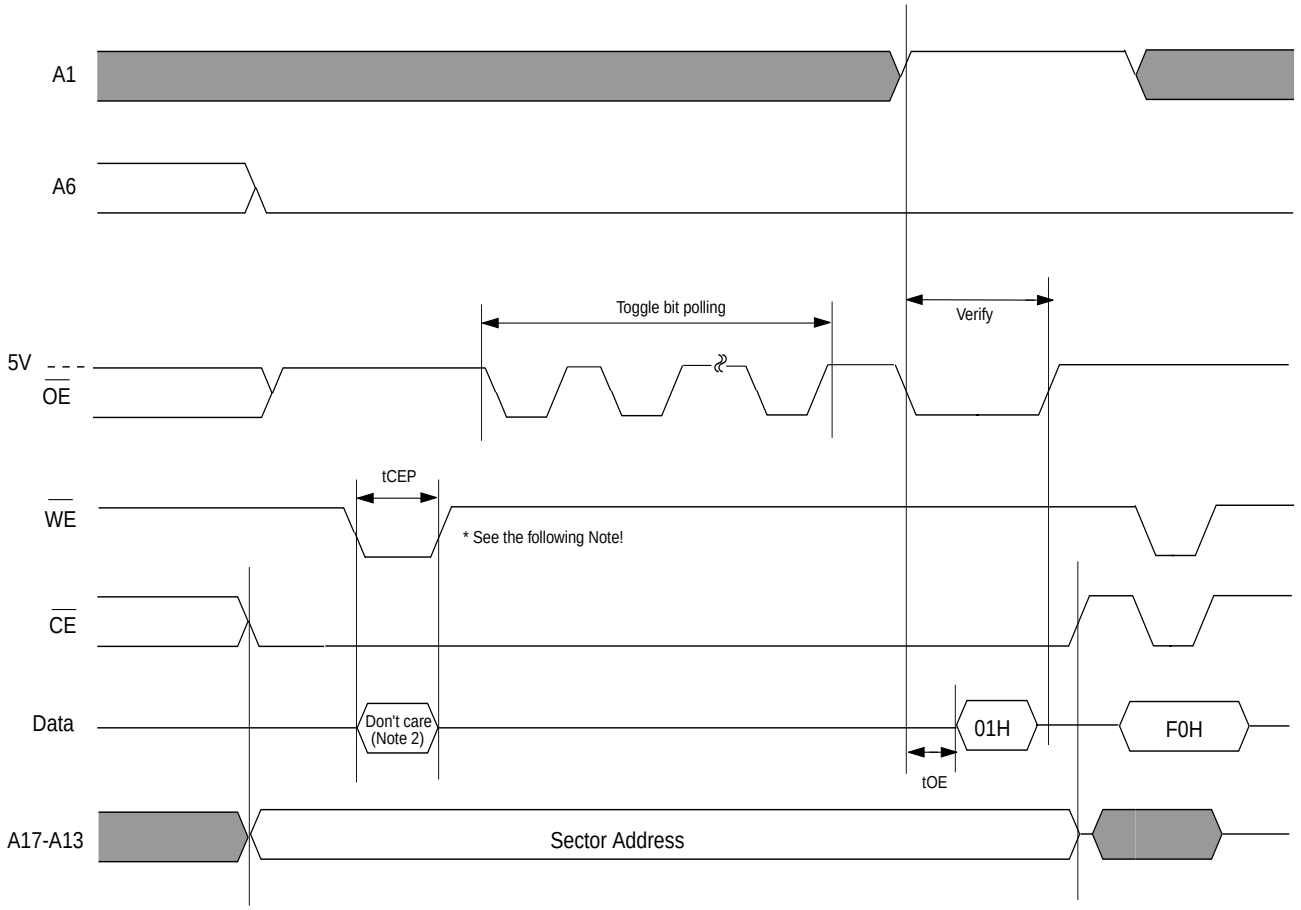


## CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITH 12V




* It is recommended before unprotect the whole chip, all sectors should be protected in advance.

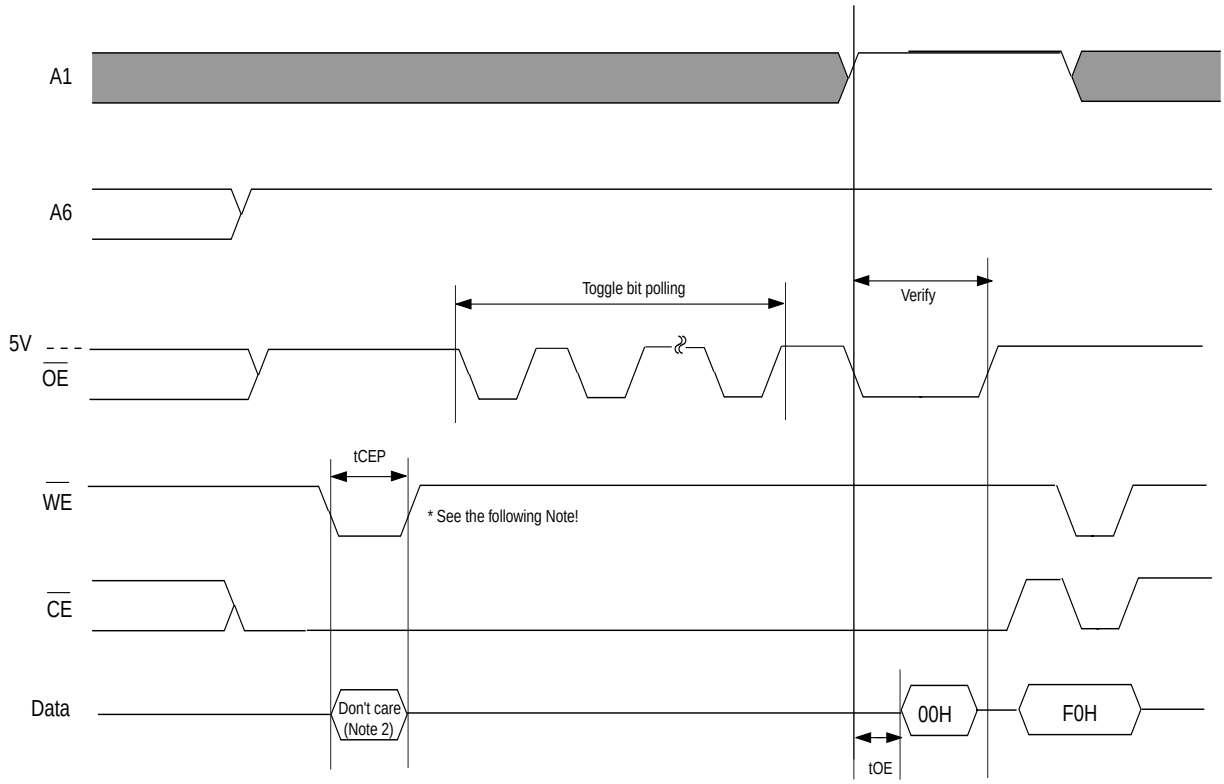
## TIMING WAVEFORM FOR SECTOR PROTECTION FOR SYSTEM WITHOUT 12V




Note1: Must issue "unlock for sector protect/unprotect" command before sector protection for a system without 12V provided.

Note2: Except F0H

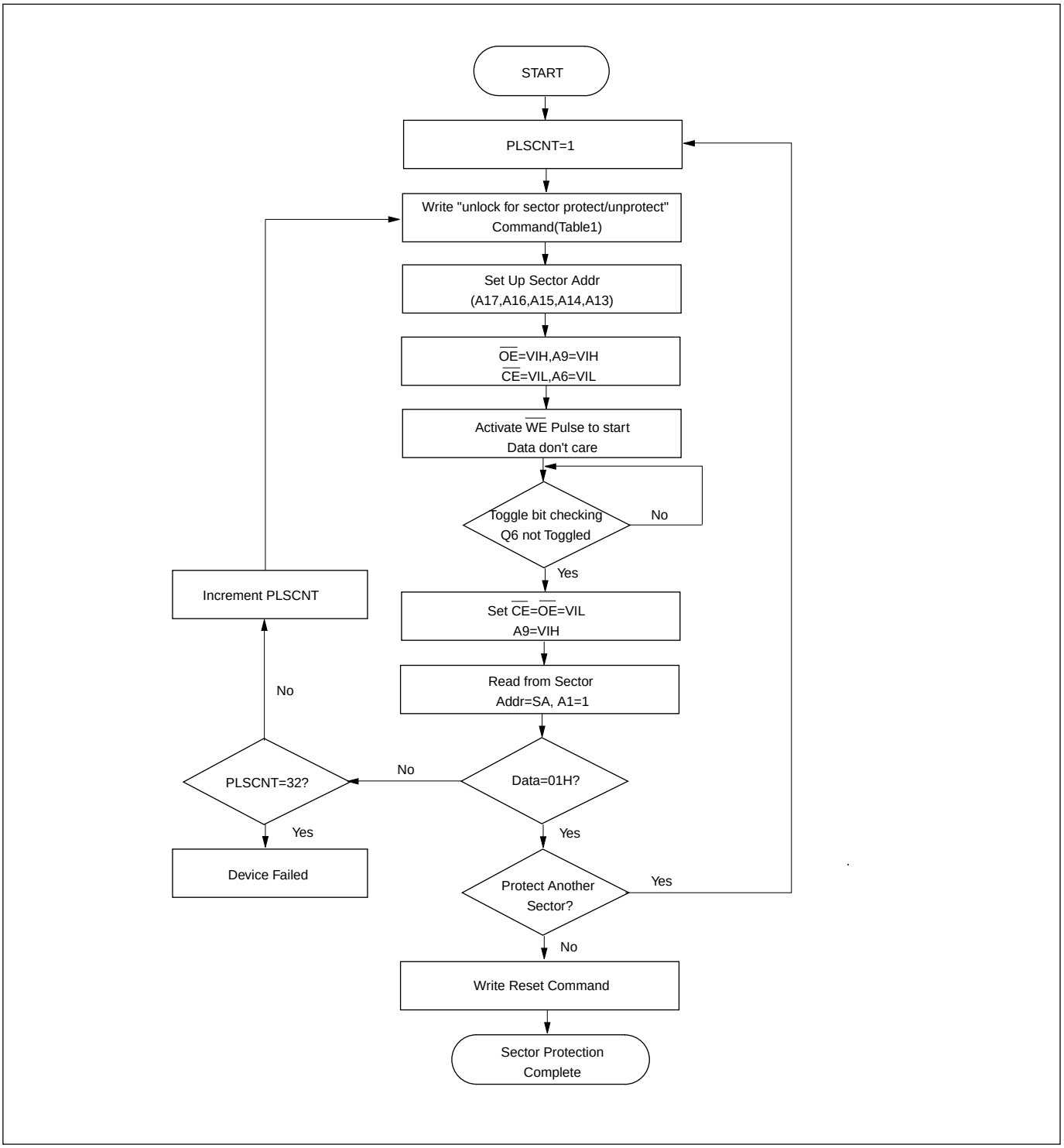
## TIMING WAVEFORM FOR CHIP UNPROTECTION FOR SYSTEM WITHOUT 12V



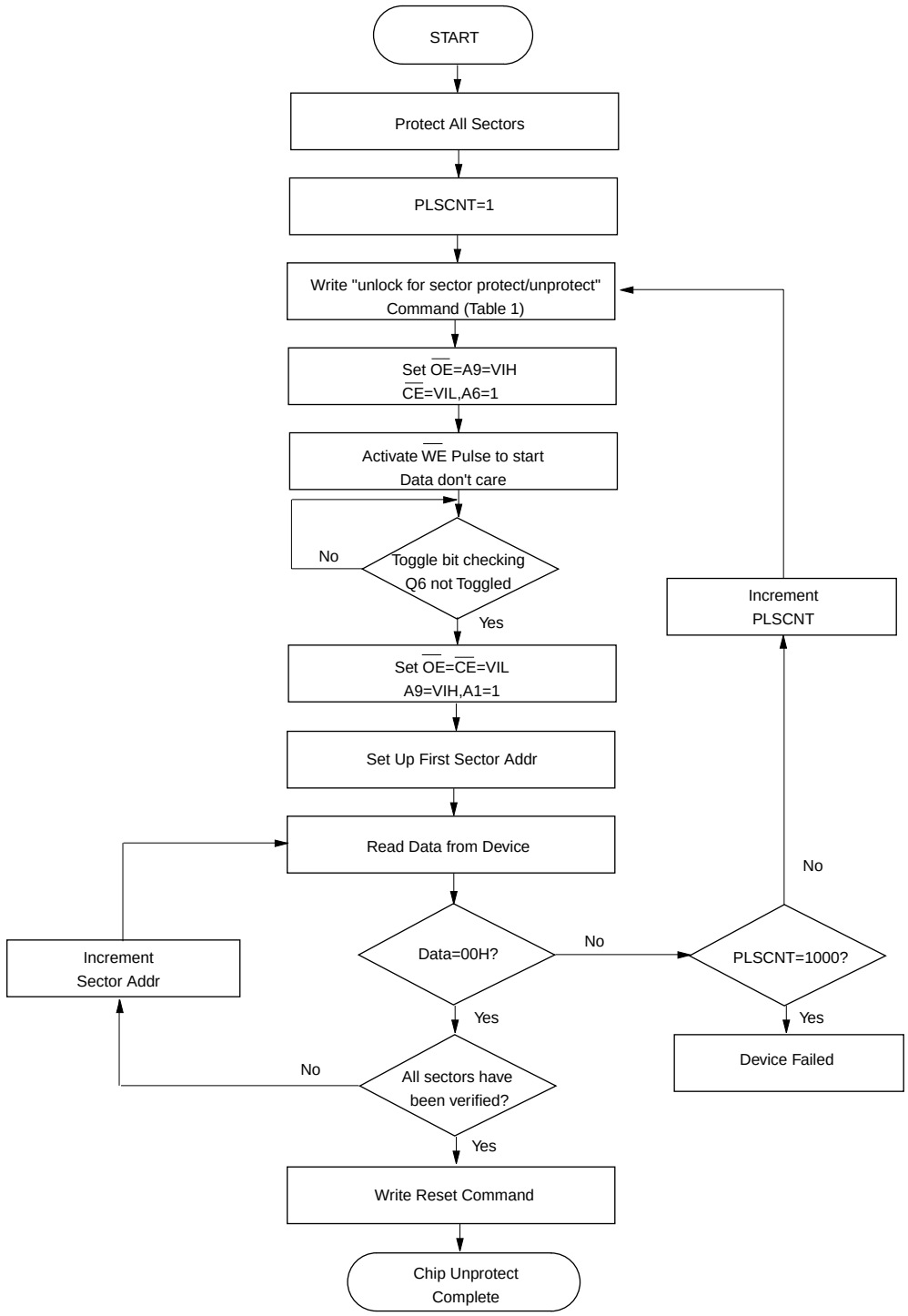

Note1: Must issue "unlock for sector protect/unprotect" command before sector unprotection for a system without 12V provided.

Note2: Except F0H

## SECTOR PROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V

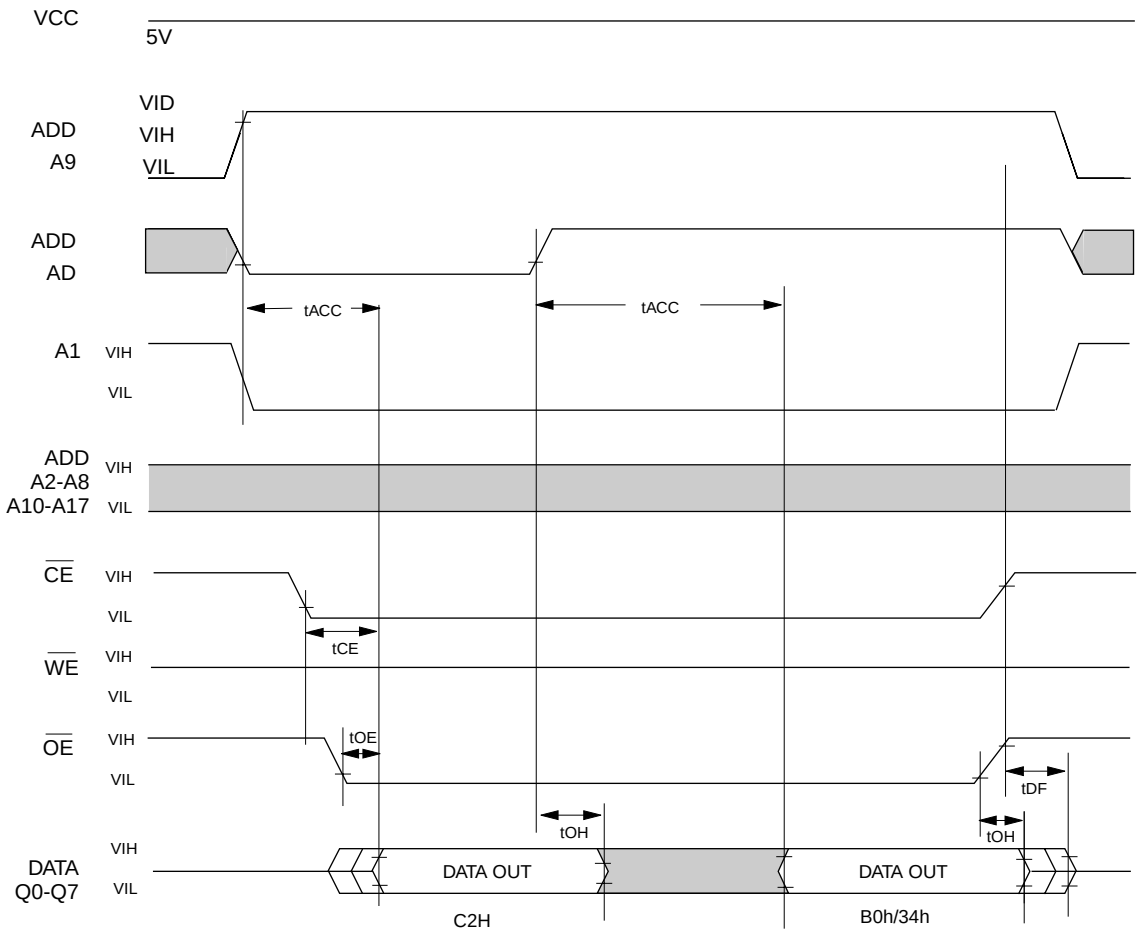


## CHIP UNPROTECTION ALGORITHM FOR SYSTEM WITHOUT 12V




* It is recommended before unprotect the whole chip, all sectors should be protected in advance.

## ID CODE READ TIMING WAVEFORM MODE



## ORDERING INFORMATION

### PLASTIC PACKAGE

| PART NO. | Access Time (ns) | Operating Current (mA) | Standby Current MAX.(uA) | Temperature Range | PACKAGE |
|---|---|---|---|---|---|
| MX29F002TPC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002TPC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002TPC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002TPC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002TTC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002TTC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002TTC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002TTC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002TQC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002TQC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002TQC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002TQC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002BPC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002BPC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002BPC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002BPC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002BTC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002BTC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002BTC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002BTC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002BQC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002BQC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002BQC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002BQC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NTPC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NTPC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NTPC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NTPC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NTTC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |

| PART NO. | Access Time (ns) | Operating Current (mA) | Standby Current MAX.(uA) | Temperature Range | PACKAGE |
|---|---|---|---|---|---|
| MX29F002NTTC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002NTTC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002NTTC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002NTQC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NTQC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NTQC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NTQC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NBPC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NBPC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NBPC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NBPC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PDIP |
| MX29F002NBTC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002NBTC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002NBTC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002NBTC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin TSOP (Normal Type) |
| MX29F002NBQC-55 | 55 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NBQC-70 | 70 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NBQC-90 | 90 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002NBQC-12 | 120 | 30 | 5 | 0°C~70°C | 32 Pin PLCC |
| MX29F002TPI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002TPI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002TPI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002TTI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002TTI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002TTI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| IMX29F002TQI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002TQI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002TQI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| IMX29F002BPI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002BPI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002BPI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |

| PART NO. | Access Time (ns) | Operating Current (mA) | Standby Current MAX.(uA) | Temperature Range | PACKAGE |
|---|---|---|---|---|---|
| IMX29F002BTI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002BTI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002BTI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002BQI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002BQI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002BQI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002NTPI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002NTPI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002NTPI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002NTTI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002NTTI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002NTTI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002NTQI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002NTQI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002NTQI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002NBPI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002NBPI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002NBPI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PDIP |
| MX29F002NBTI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002NBTI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002NBTI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin TSOP (Normal Type) |
| MX29F002NBQI-70 | 70 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002NBQI-90 | 90 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |
| MX29F002NBQI-12 | 120 | 45 | 5 | -40°C~85°C | 32 Pin PLCC |

## ERASE AND PROGRAMMING PERFORMANCE(1)

| PARAMETER | LIMITS | | | UNITS |
|---|---|---|---|---|
| | MIN. | TYP.(2) | MAX.(3) | |
| Sector Erase Time | | 1 | 8 | s |
| Chip Erase Time | | 3 | 24 | s |
| Byte Programming Time | | 7 | 210 | us |
| Chip Programming Time | | 3.5 | 10.5 | sec |
| Erase/Program Cycles | 100,000 | | | Cycles |

Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25℃, 5V.
3.Maximum values measured at 25℃, 4.5V.

## LATCHUP CHARACTERISTICS

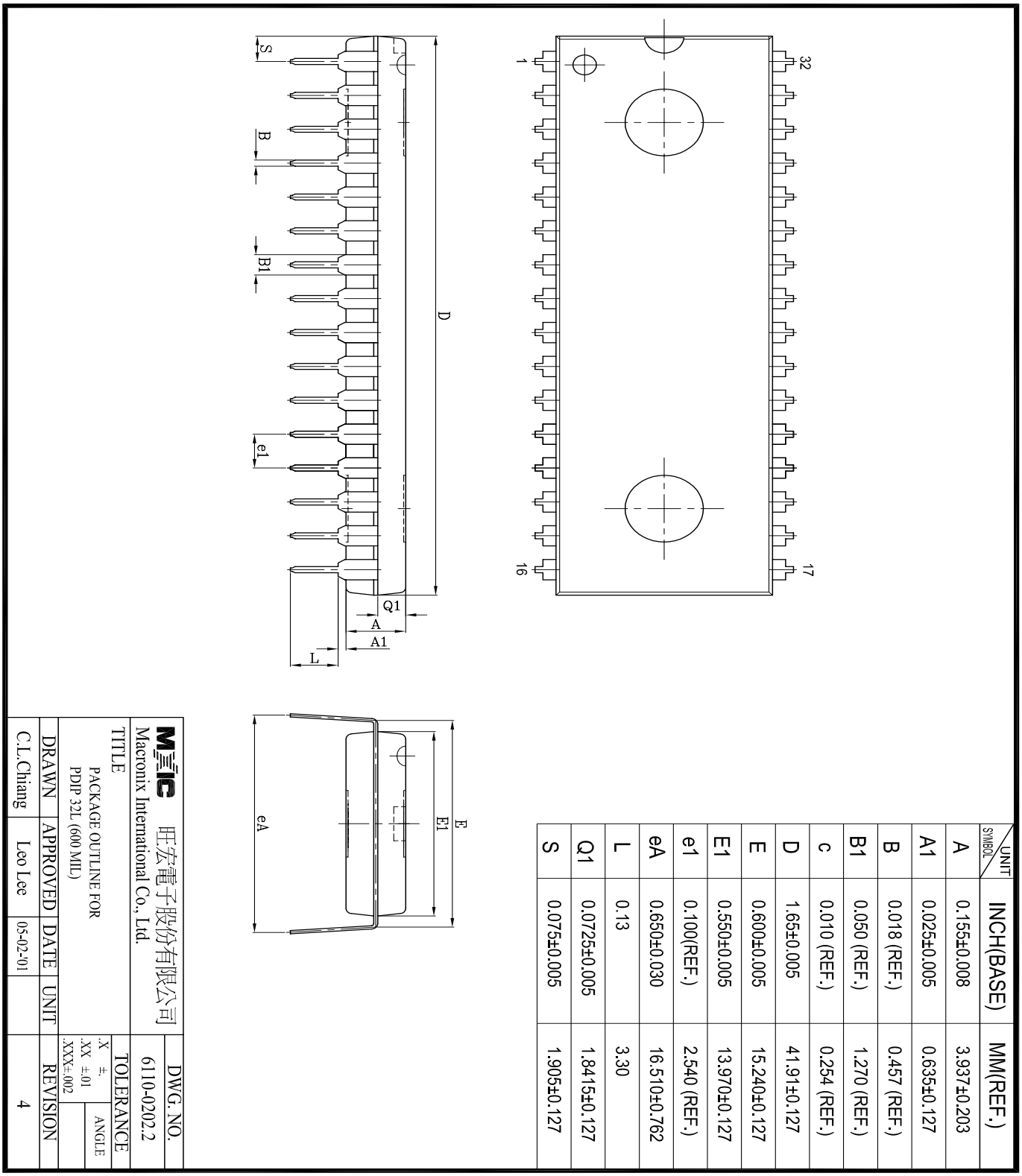
| | MIN. | MAX. |
|---|---|---|
| Input Voltage with respect to GND on all pins except I/O pins | -1.0V | 13.5V |
| Input Voltage with respect to GND on all I/O pins | -1.0V | Vcc + 1.0V |
| Current | -100mA | +100mA |
| Includes all pins except Vcc. Test conditions: Vcc = 5.0V, one pin at a time. | | |

## DATA RETENTION

| PARAMETER | MIN. | UNIT |
|---|---|---|
| Data Retention Time | 20 | Years |

## PACKAGE INFORMATION

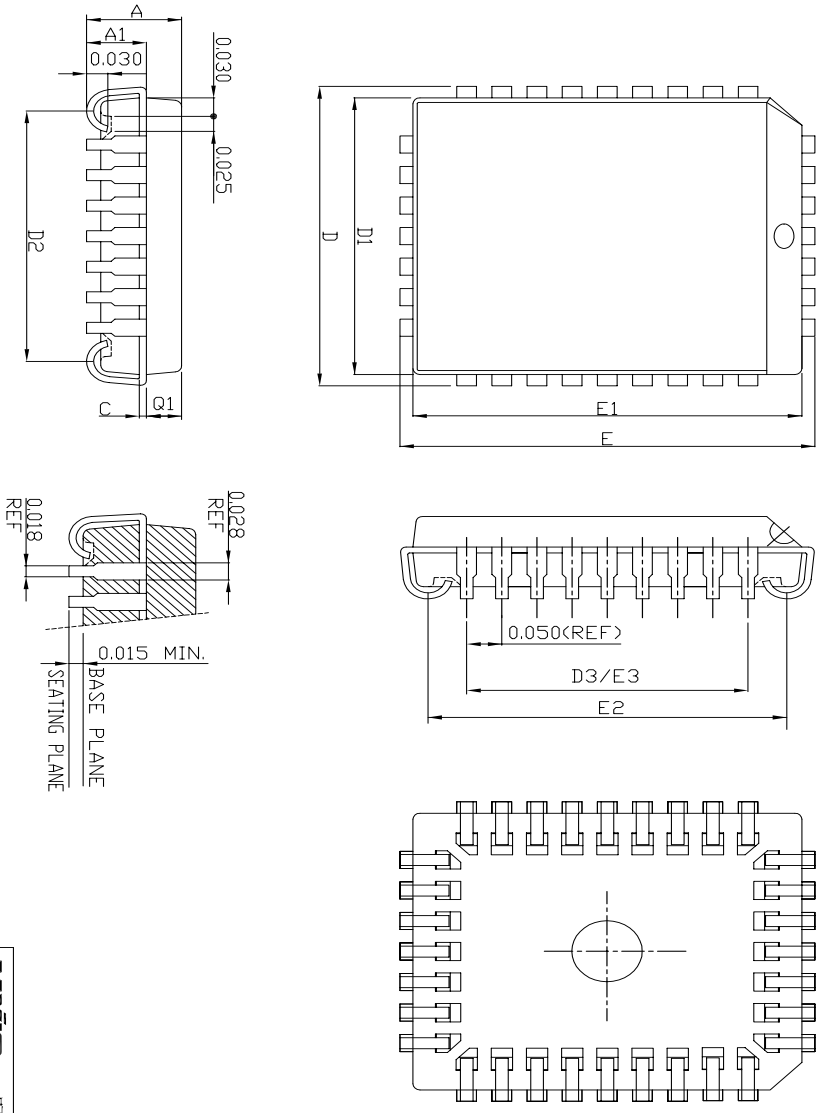
### 32-PIN PLASTIC DIP




| SYMBOL / UNIT | INCH(BASE) | MM(REF.) |
|---|---|---|
| A | 0.155±0.008 | 3.937±0.203 |
| A1 | 0.025±0.005 | 0.635±0.127 |
| B | 0.018 (REF.) | 0.457 (REF.) |
| B1 | 0.050 (REF.) | 1.270 (REF.) |
| c | 0.010 (REF.) | 0.254 (REF.) |
| D | 1.65±0.005 | 41.91±0.127 |
| E | 0.600±0.005 | 15.240±0.127 |
| E1 | 0.550±0.005 | 13.970±0.127 |
| e1 | 0.100(REF.) | 2.540 (REF.) |
| eA | 0.650±0.030 | 16.510±0.762 |
| L | 0.13 | 3.30 |
| Q1 | 0.0725±0.005 | 1.8415±0.127 |
| S | 0.075±0.005 | 1.905±0.127 |

| | | | | |
|---|---|---|---|---|
| MXIC 旺宏電子股份有限公司 Macronix International Co., Ltd. | | | | DWG. NO. 6110-0202.2 |
| TITLE PACKAGE OUTLINE FOR PDIP 32L (600 MIL) | | | UNIT | TOLERANCE .X ±. .XX ±.01 .XXX±.002 ANGLE |
| DRAWN | APPROVED | DATE | | REVISION |
| C.L.Chiang | Leo Lee | 05-02-'01 | | 4 |

## 32-PIN PLASTIC LEADED CHIP CARRIER (PLCC)

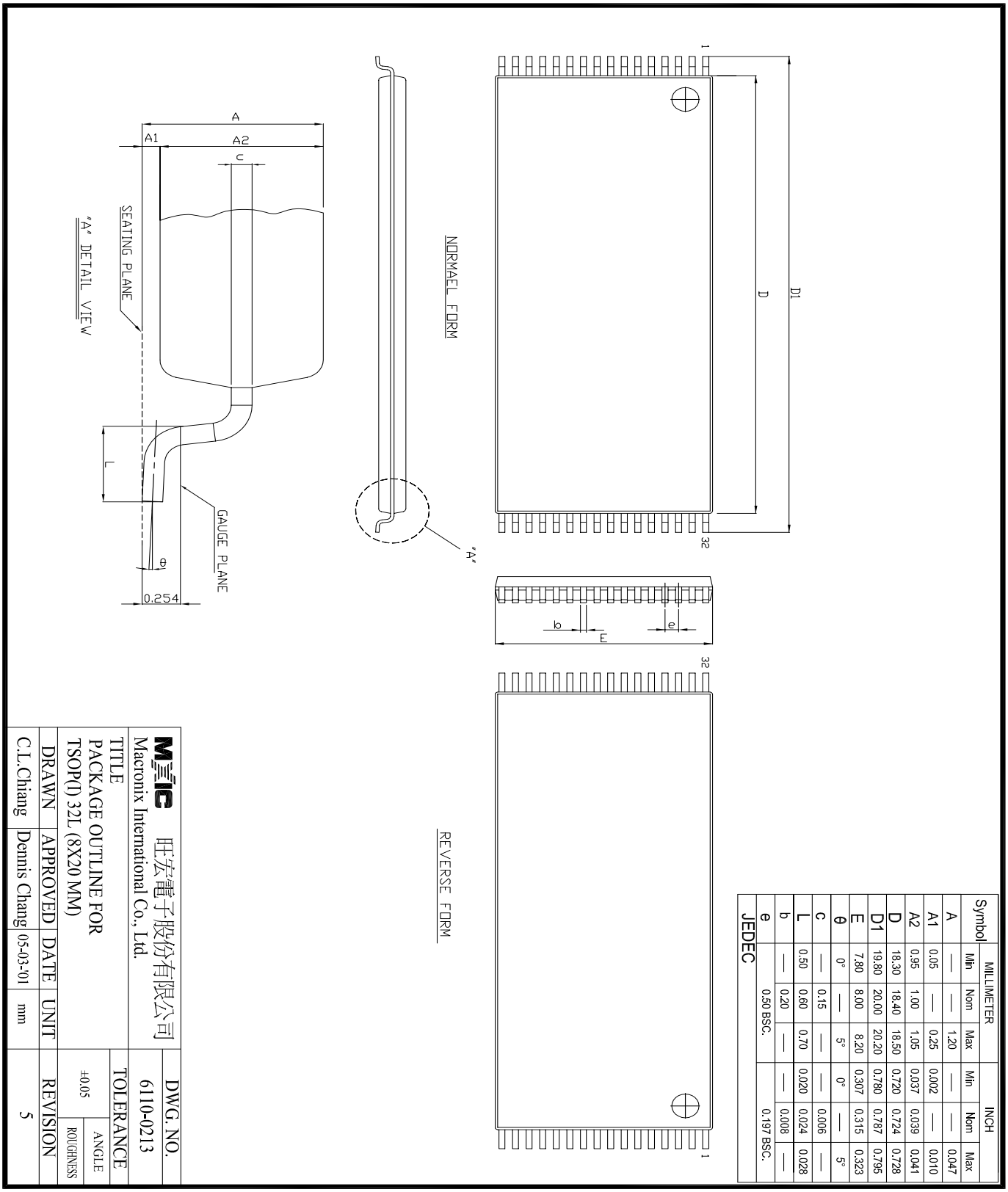



| Symbol | Dimension in inch (Ref.) | | | Dimension in mm (Base) | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | | | 0.140 | | | 3.56 |
| A1 | 0.080 | 0.085 | 0.090 | 2.03 | 2.16 | 2.29 |
| Q1 | 0.048 | 0.050 | 0.052 | 1.22 | 1.27 | 1.32 |
| c | | 0.010(REF) | | | 0.25(REF) | |
| D | 0.485 | 0.490 | 0.495 | 12.32 | 12.45 | 12.57 |
| D1 | 0.450 | 0.453 | 0.456 | 11.43 | 11.51 | 11.58 |
| D2 | 0.400 | 0.410 | 0.420 | 10.16 | 10.41 | 10.67 |
| D3 | | 0.300(REF) | | | 7.62(REF) | |
| E | 0.585 | 0.590 | 0.595 | 14.86 | 14.99 | 15.11 |
| E1 | 0.550 | 0.553 | 0.556 | 13.97 | 14.05 | 14.12 |
| E2 | 0.500 | 0.510 | 0.520 | 12.70 | 12.95 | 13.21 |
| E3 | | 0.400(REF) | | | 10.16(REF) | |

REFERENCE DOCUMENT : JEDEC SPEC - MS-016a

| | | | | | |
|---|---|---|---|---|---|
| 旺宏電子股份有限公司 Macronix International Co., Ltd. | | | | DWG. NO. | |
| | | | | 6110-0209.1 | |
| TITLE | | | | TOLERANCE | |
| PACKAGE OUTLINE FOR PLCC 32L | | | | .X ± .XX ±.01 .XXX±.002 | ANGLE ±2° |
| DRAWN | APPROVED | DATE | UNIT | REVISION | |
| C.L.Chiang | Dennis Chang | 05-03-'01 | inch | 2 | |

## 32-PIN PLASTIC TSOP




| Symbol | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | — | — | 1.20 | — | — | 0.047 |
| A1 | 0.05 | — | 0.25 | 0.002 | — | 0.010 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| D | 18.30 | 18.40 | 18.50 | 0.720 | 0.724 | 0.728 |
| D1 | 19.80 | 20.00 | 20.20 | 0.780 | 0.787 | 0.795 |
| E | 7.80 | 8.00 | 8.20 | 0.307 | 0.315 | 0.323 |
| θ | 0° | — | 5° | 0° | — | 5° |
| c | — | 0.15 | — | — | 0.006 | — |
| L | 0.50 | 0.60 | 0.70 | 0.020 | 0.024 | 0.028 |
| b | — | 0.20 | — | — | 0.008 | — |
| e | | 0.50 BSC. | | | 0.197 BSC. | |
| JEDEC | | | | | | |

| | | | |
|---|---|---|---|
| MIC 旺宏電子股份有限公司 | | | DWG. NO. |
| Macronix International Co., Ltd. | | | 6110-0213 |
| TITLE | | | TOLERANCE |
| PACKAGE OUTLINE FOR | | | ANGLE ±0.05 |
| TSOP(I) 32L (8X20 MM) | | | ROUGHNESS |
| DRAWN | APPROVED | DATE | UNIT |
| C.L.Chiang | Dennis Chang | 05-03-'01 | mm |
| | | | REVISION |
| | | | 5 |

## REVISION HISTORY

| Revision | Description | Page | Date |
|---|---|---|---|
| 1.0 | 1.To remove "Advanced Information" datasheet marking and contain information on products in full production | P1 | DEC/27/1999 |
| | 2.The modification summary of Revision 0.9.8 to Revision 1.0: | | |
| | 2-1.Program/erase cycle times:10K cycles-->100K cycles | P1,46 | |
| | 2-2.To add data retention 20 years | P1,46 | |
| | 2-3.To add industrial grade range from "Read Mode" to "Full Range" | P17,19,21,41-43 | |
| | 2-4.To remove A9 from "timing waveform for sector protection for system without 12V" | P36 | |
| | To remove A9 from "timing waveform for chip unprotection for system without 12V" | P37 | |
| | 2-5.Multi-sector erase time-out:30ms-->30us, tBAL:80us-->100us | P8,20,21 | |
| 1.1 | To modify "Package Information" | P45~47 | JUN/14/2001 |

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**http : //www.macronix.com**